DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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APPLICATION SPECIFIC INTEGRATED CIRCUIT

Inside this issue:

An Integrated Circuit (IC) designed for a particular use and not for general use is called an Application- Specific Integrated Circuit (ASIC). It is basically an integrated circuit designed specifically for a special purpose or application. Application specific integrated circuits provide their users the ability to manufacture products having a proper design. Many different ASIC technologies are available, including gate array, standard cell, full custom design, and programmable logic devices. The ASIC forms, in a single, semi-conductor substrate, the equivalent of several different integrated circuits each designed to perform one or more desired operations, such as a microprocessor operation, a memory operation, various interface operations (e.g., memory interface, processor interface), etc.

ASIC operational blocks are typically designed to include thousands of individual logic gates necessary for performing the desired operation(s) An example of this is a chip which is designed only to run a cell phone. Whereas there are 7400 series and 4000 series integrated circuits as logic building blocks which can be w ired together and used in various applications.

Application specific integrated circuits (ASICs) can consolidate the work of many chips into a single, smaller, faster package, reducing manufacturing and support costs while boosting the speed of the device built with them. Designers prefer using application specific integrated circuits as it lets them use the power of constantly improving silicon technology to build devices targeted at specific functions, such as routing. Modern application specific integrated circuit chips often include entire 32-bit processors and other large building-locks. This type of ASIC chip is often referred to as a system-on-a-chip (SoC). Design flow of ASIC chips is highly automated.

EXAMPLES OF ASIC

Examples of ASIC's include:

- An IC that encodes and decodes digital data using a proper encoding/ decoding algorithm.
- A medical IC designed to monitor a specific human biometric parameter.
- An IC designed to serve a special function within a factory automation system.
- An amplifier IC designed to meet certain specifications not available in standard amplifier products.
- A proprietary system-on-a-chip (SOC).
- An IC that's custom-made for a particular automated test equipment.

DESIGNING OF ASIC

ASIC design can be divided into following sections: register-transfer level (RTL) description, simulation, syntheses, extraction, and physical verification. A hierarchy of programmable interconnects allows the logic blocks of an FPGA ASIC chip to be interconnected, similar to a one-chip programmable breadboard. The logic blocks interconnected then can be programmed so that the FPGA ASIC chip can perform whatever logical function is needed.

A structured ASIC provides reduced entry cost and f aster time by using a predefined arrangement of late-stage, mask-customizable logic and predif-fused macros and IP. With the integration of increasing system components on single ASIC chips, the complexity of ASIC prototyping is increased. System design involves complex layout issues. Specifications of cells are provided by the vendors in form of a technology library which contains information about geometry, delay, and power characteristics of cells. ASIC chips are designed and manufactured to meet most industry specifications.

TYPES OF ASIC:

1. Cell Based Application Specific Integrated Circuits (ASICS) Benefits:

- Highest performance, power and integration.
- Cell-based ASICs are offered with a selection of IP cores.
- Perfect for high-volume designs that require the highest density and performance.
- available in a range of process technologies
- Max. clock speed: Up to 1 GHz
- Memory: High-density SRAM and embedded DRAM
- Signal I/Os: Up to 1400
- Usable ASIC gates: Up to 100M
- Featured IP: ARM CPUs, Tensilica CPUs and DSPs, USB 2.0, eDRAM, SerDes, PCI Express, SATA/SAS, SPI4.2.

IPCORE

There are a large number of IP cores in cell-based ICs, including CPU cores and analog logic cores. Customers are supported in their own system chip design development by these options.

Core List

- Digital Core
- Analog Core
- SRAM
- eDRAM
- I/O

Services Provided During Cell-Based I Development Linked processes from logic design to manufacturing features in production of cell-based ICs helps in providing an environment for short turnaround time in mass-producing large-scale integration, advanced performance, and low power consumption.

Benefits

- Logic design taking layout design into account at an early stage.
- Layout design taking manufacturing (DFY or DFM) into account.
- Test design improving manufacturing quality.
- Feedback from manufacturing to logic design and test design.

2. Gate Array & Embedded Array ASICs

Gate arrays help reduce the cost, turn round time and risk while improving power consumption, EMI and performance. These arrays, based on a sea-of-gates architecture, which is customized using only the metallization layers for interconnect. Low NRE costs and fast turnaround time are its results.

HIGHLIGHTS

- From the #1 supplier worldwide, with over 750 tape-outs over the past 3 years.
- Low price, low NRE cost (as low as $10,000), easy-to-design option, easy Logic consolidation due to small gate counts and small package design.
- FPGA-compatible packages also

available. In just nine short days from tape out, we can have engineering samples ready to go.

- Max. clock speed: 133 MHz
- Memory: Diffused and metalized SRAM
- Signal I/Os: From 20 to 876
- Usable ASIC Gates: From 1.5K to 1.6M

- Featured IP: DMA controller, interrupt controller, PCI controller, DPLL, UART, timer, parallel interface unit, UART + FIFO, Tensilica CPUs and DSPs
- Master slices: 158

3. EDRAM Application Specific Integrated Circuits (ASICS)

Following are some of the features that make eDRAM, the ideal solution for a wide variety of applications-

- Random access time an order of magnitude shorter than competitor offerings.
- Fully CMOS-compatible process using a single fab and few extra masks to minimize cost
- SRAM-like access for easy integration with existing intellectual property (IP)
- SoC-friendly macros that simplify integration, with orientation in any direction and over-the-top routing The latest 55 nm family, which adds significant process enhancements to the improved materials that have proven so successful in our previous 90 nm family.

APPLICATIONS

These characteristics have helped fuel the growing popularity of eDRAM for a variety of applications – from communications systems to home electronics, from enterprise servers to entertainment systems. The success complex system LSI chip for the Nintendo Wii™ and Microsoft® Xbox 360™ has propelled fabrication volume to many millions of devices.

FUTURE ASPECTS

If it is used in proper way or manner then it can proved as a boon To the whole world as it is already proving its importance in the field of satellite and radar systems.

Design by

T.Kamesh

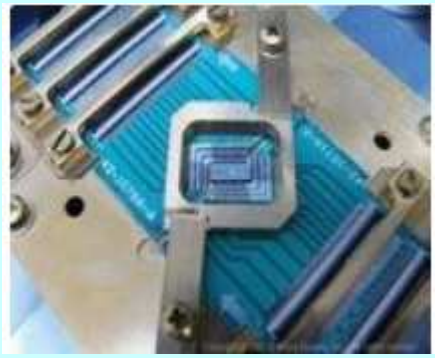
CAM: Memory faster than RAM

CAMS (CONTENT ADDRESSABLE MEMORIES)

In their most trivial form, work in a way opposite to conventional memory. Effectively a cam is a searching tool that looks for the data in question within a database. A CAM commonly work as hardware search engines in routers and switches to accelerate forwarding of packet on the destination root.CAM i.e. Content Addressable Memory stores data in a similar fashion to a conventional RAM. However, "reading" the CAM involves providing input data to be matched, then searching the CAM for a match so that the address of the match can be provided to output. Typical applications of CAM are networking, telecom (e.g., ATM cells), and consumer.

CAM ARCHITECTURE

Writing to a CAM is exactly like writing to a conventional RAM. However, the "read" operation is actually a search of the CAM for a match to an input "tag." In addition to storage cells, the CAM requires on e or more comparators Architectures can also include an input address bus. Another common scheme involves writing to consecutive locations of the CAM as new data is added. The outputs are a MATCH signal and either an encoded N-bit value or a one-hot -encoded bus with one match bit corresponding to each CAM cell. The multi-cycle CAM architecture tries to find a match to the input data word by simply sequencing thro ugh all memory locations – reading the contents of each location, comparing the contents to the input value, and stopping when a match is found . At that point, MATCH and MATCH_VALID are asserted. If no match is found, MATCH is not asserted, but MATCH_VALID is asserted after all addresses are compared. MATCH_ VALID indicates the end of the read cycle. In other words, MATCH_VALID asserted and MATCH not asserted indicate that all the addresses have been compared during a read operation and no matches were found .When a match is found, the address of the matching data is provided as an output and the MATCH signal is asserted. It is possible that multiple locations might contain matching data, but no checking is done for this. Storage for the multi-cycle CAM ca n be either in distributed RAM (registers) or block RAM. In the single-cycle CAM architecture, there is



a comparator for each storage Location. If there are N CAM locations, the output is a single N-bit MATCH signal, which represents the one-hot encoding of the comparator results at each location. A '1' indicates a match and a '0' represents no match. Note that a match at an y location triggers assertion of the MATCH signal; no checking is done multiple addresses, which contain matching data. The storage cells are implemented as distributed registers. For the single-cycle CAM generators, you can choose to have a single MATCH output, which is the logical OR of all of the MATCH bit.

FUNCTIONS OF CAMS

In order to get a true understanding of the functionality cam ,you need to dig a little deeper into the domain these works .if you look at either the OSI reference model or the TCP /IP stack ,you will find that the lowers three layers are the ones that are concern with the packet delivery to its peer, while all other layers are more concerned with the content, its presentation and formatting another importance task that needs to be performed by these upper layers i s to ensure delivery of the packet to its correct recipient . This is done in two ways1-usin g MAC (media access control)address2- using IP address.

TYPES OF CAMS

Fundamentally, CAMs are of two types: binary and ternary. As it indicates, a binary CAM has two bit states, while a ternary CAMs has 1, 0 and a third state called "don't care ." So search-hit on a binary CAM could be an exact match or a partial match. Currently ternary CAMs are de-facto in the industry. These bring the possibility of multiple match in a look up table. All the access list (ACI) tables for packet forwarding use a popular address resolution algorithm called the longest prefix match where the addresses are placed in the CAM based on certain priorities and the CAM by itself has a priority encoder that helps in resolving the winning address.

In the context two sets of data world appear for a single entry in the table. One referring to the data to be looked up for and the other referring to the mask that is to be applied on every bit during look up. The convention used with respect to the mask in this context is "A'1' refers to data masked and a '0' refers to data not being masked". The possibility of masking off of certain bits of the data opens up a wide range of applications were partial match is necessary for in stance, at the edge of a router, where the router only worries about the destination network address and not the host ID.

IMPLEMENTATION AND PERFORMANCE/ UTILIZATION :

The implementation is mostly behavioral, but key blocks are implemented structurally to target features of Actel devices. Both architectures are implemented in VHDL. Generics allow setting the number of address bits, the memory depth and width , and the degree of parallelism.

To make the simulation easier to follow, the data written to a given address is the address itself. Four writes occur.

APPLICATIONS OF CAM

Implication of ARP-when a new host gets associated with a network the foremost thing that the network processor does is to update it s network database with the MAC and IP address of the new host.

This update taken place in CAM table. 2-signature recognition-with t he performance and speeds that current technologies are achieving in communication, the performance of CAM is extremely important. One of the foremost applications that the Internet needs is data protection. With new ways coming in vogue to hack an end point, the need for protection from such attacks, be it through a virus or a spam, is necessary. If such a process can be achieved in hardware, it improves the throughput drastically. CAMs can help in such a cause by maintaining a signature data base and an associate processor can scan the packets for such signatures and drop packets if necessary; such a functionality would add immense value to the content moved across the Inter net .

WAY FORWARD

CAMs, as seen above, are becoming an important tool in the communications arena and any research towards further improving their value by enhancing their throughput or reducing the cost would add to the advantage.

CAMs, as seen above, are becoming an important tool in the communications arena and any research towards further improving their value by enhancing their throughput or reducing the cost would add to the advantage.

EXAMPLE APPLICATIONS

Content-addressable memory is often used in computer networking devices. For example, when a network switch receives a data frame from one of its ports, it updates an internal table with the frame's source MAC address and the port it was received on. It then looks up the destination MAC address in the table to determine what port the frame needs to be forwarded to, and sends it out on that port. The MAC address table is usually implemented with a binary CAM so the destination port can be found very quickly, reducing the switch's latency.

Ternary CAMs are often used in network routers, where each address has two parts: the network address, which can vary in size depending on the subnet configuration, and the host address, which occupies the remaining bits. Each subnet has a network mask that specifies which bits of the address are the network address and which bits are the host address.

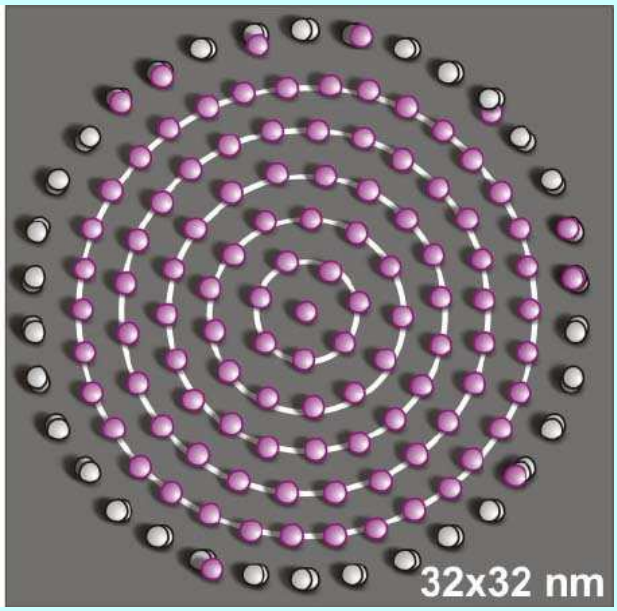
Routing is done by consulting a routing table maintained by the router which contains each known destination network address, the associated network mask, and the information needed to route packets to that destination. Without CAM, the router compares the destination address of the packet to be routed with each entry in the routing table, performing a logical AND with the network mask and comparing it with the network address.

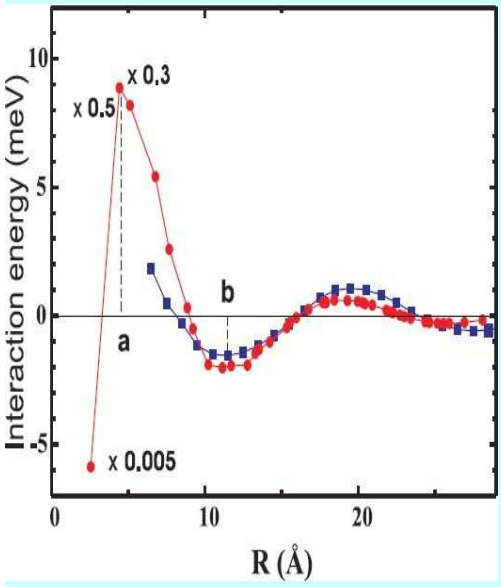
If they are equal, the corresponding routing information is used to forward the packet. Using a ternary CAM for the routing table makes the lookup process very efficient. The addresses are stored using "don't care" for the host part of the address, so looking up the destination address in the CAM immediately retrieves the correct routing entry; both the masking and comparison are done by the CAM hardware. This works if (a) the entries are stored in order of decreasing network mask length, and (b) the hardware returns only the first matching entry; thus, the match with the longest network mask (longest prefix match) is used.This update taken place in CAM table. 2-signature recognition-with t he performance and speeds that current technologies are achieving in communication, the performance of CAM is extremely important Routing is done by consulting a routing table maintained by the router which contains each known destination .

Design by
T.Rohith

Quantum Mirage

Since it first appeared on the cover of Nature in February 2000, the “quantum mirage" has featured on posters, calendars, websites and the covers of various books and magazines. The image - which was obtained using a scanning tunneling microscope - shows the electronic wave functions inside an elliptical "quantum corral" made of cobalt atoms on a copper surface. It was created by Hari Manoharan, Christopher Lutz and Don Eigler of the IBM Almaden Rese arch Center in California. In 1990, working with Erhard Schweizer, Eiger spelt out the letters "IBM" using 35 xenon atoms. And three years later, working with Lutz and Michael Crommie, he released the first images of the "quantum corral", which have also been reproduced in numerous places.





All moving particles have a wavelike nature. This is rarely significant on an everyday scale. But in atomic dimensions, where distances are measured in nanometers, moving particles behave like waves. This phenomenon is what makes the electron microscope workable. It is of interest to researchers in nanotechnology, who are looking for ways to deliver electric currents through circuits too small for conventional wiring.

he term quantum mirage refers to a phenomenon that may make it possible to transfer data without conventional electrical wiring. Instead of forcing charge carriers through solid conductors, a process impractical on a microscopic scale, electron wave phenomena are made to produce effective currents. A quantum mirage is a peculiar result in quantum chaos. Every system of quantum dynamical billiards will exhibit an effect called scarring, where the quantum probability density shows traces of the paths a classical billiard ball would take. For an elliptical arena, the scarring is particularly pronounced at the foci, as this is the region where many classical trajectories converge.

The scars at the foci are colloquially referred to as the "quantum mirage". They are two dimensional structures built atom by atom (using approximately 30-80 atoms) on atomically smooth metallic surfaces using a scanning tunneling microscope (STM). Once the corrals are built, the e STM can be used to study these nanometer scale structures with atomic resolution in space and better than meV (micro electron Volt) resolution in energy. The data of the STM can be rendered in false color to pro duce breathtaking images that reveal standing wave patterns of coherent electrons inside the corrals. The presence or absence of a quantum mirage might be used t o represent one bit of data in a region far smaller than any current electronic device can manage. It has the potential to enable data transfer within future Nano-scale electronic circuits so small that conventional wires do not work. IBM scientists are hoping to use quantum mirages to construct atomic scale processors in the future.

Design by

V.Bharath

Common Admission Test (CAT)

The common admission test (CAT) is an All India test conducted by the Indian Institutes of management (IIMs) as an entrance exam for the management programmers of its 14 B (Business) schools. About 250,000 students took CAT 2008 for about 1500 seats in the IIMs more selective than the universities. The CAT is the first step for admission to the IIMs. After the test, by the second week of January next year, the IIMs declare exam sc ores and put up a list of candidates who are eligible for the next stag e of a group discussion for some IIMs & an individual interview.

CAT 2009: The first ever computer based CAT conducted by prometric during 28th nov - 7th dec. Many other business Schools in India, other than IIMs, also accept the CAT scores for admission. This has contributed to the CAT gaining an extremely high popularity. As of 2008, CAT scores are accepted by approximately 120 MBA institutes in India.

WHY CAT ?

- CAT is the only exam which provides entrance in the top B-schools of India in spite of IIMs. CAT also does not require any technical background like other exams required. It requires only 8th to 10tn class math's for its quantitative section. So, some of the point s why we select CAT are CAT is not about following rules, it is all about breaking the rules.
- CAT is not about rocket science, it is about the basics of life.
- CAT is not about taken tracks, it is about defining a new track.
- CAT is not about selecting answers, it is about eliminating the answer.

HOW TO PREPARE FOR CAT?

This is a very complex question that how we prepare for CAT. So, the answer is here. Many of us thought that CAT is a test of your managerial aptitude & managerial skills like:

- Time management
- How would handle pressure & uncertainty.
- Decision making.

Remember, CAT is not solving 150 questions in 120 minutes. It is about solving 90 to 95 questions with 85 to 90 % accuracy. Here are a few tips that would help to fetch you a call from the best B-schools in the country.

TIP 1: HANDLE PRESSURE AND UNCERTAINTY WELL

Handling pressure and uncertainty is a crucial element of CAT. This is a essential skill that a manager requires in his/her daily decision making process The CAT examination spans 120 minutes, but if you are able to handle pressure in the first 15 and last 10 minutes, your chances to excel increase. Some points to help you at this stage are:

1. Have a flexible strategy.
2. Scan your question paper for the initial three to four minutes to locate easy questions.
3. Attempt your favorite section first.
4. Remember CAT is another name of uncertainty.

TIP 2: SEQUENCE AND PRIORTISE YOUR MANTRAS FOR SUCCESS

- Deciding on the sequence in which you will attempt the various sections.
- Allocating an appropriate time for each section.
- Prioritizing questions within sections. For E.g.- your strategy before entering the examination hall should be-

1. Scanning : 3-4 minutes
2. Data Interpretation : 40 minutes
3. Verbal Ability : 40 minutes

The section may interchange according to your favorite section.

TIP 3: SOME SPECIFIC SECTION STRATEGIES

1. Quantitative ability :- Attempt question in three rounds-

Round 1:

1. Attempt all one liners
2. Attempt all two liners
3. Attempt all four liners
4. Attempt those questions in which data are given.

Round 2:

Come back to the left questions of Round 1. Under pressure, you might left some easy questions . Attempt them again.

Round 3:

If time permits, attempt the lengthier questions of your favorite topics. But remember, it takes just 5 to 10 seconds to decide whether you should attempt or leave the question.

2. Verbal ability:- Most students attempt English usage or Reading and Comprehension part first.

- In Para jumbles, look out for structural & logical connectors.
- Before attempting Reading & Comprehension, scan the question once.
- Be careful in grammatical portion.

3. Data Interpretation / Data approximation:-

- Revise your percentages & approximation.
- Data sufficiency questions are independent of each other & should be attempted first.
- After data sufficiency questions, attempt single graph questions followed by the double graph questions.
- Questions based on logical games & logical tables should be attempt at last.

COURCES OFFERED BY SOME TOP INDIAN SCHOOLS

Courses offered @ IIM Bangalore;

- PGP
- PGPPM [PGP IN PUBLICY MAKING]
- PGSEM [PG in software enterprise management,2.5 yeas part tie course for working]
- EPGP
- FPM [fellow programme in management]
- MDP [Management Development programme] Courses offered @ Indian School of Business (ISB) Hyderabad
- 1 year PGP
- Business Research Fellowship Programme (BRFP) Courses offered @ Management Deveoopent Institute (MDI) Gurgaon
- National Management Programme, NMP
- PGPPM
- PGP in Human Resource Management
- PGP in International Management
- School of Energy Management Courses offered @ Xavier Labor Research Institute (XLRI) Jamshedpur
- PGP in Business Administration.
- PGP in Personnel Management & Industrial Relations (PMIR)

Courses offered @ Faculty of Management Sciences (FMS) University Of Delhi.

Design by
V.Nihar

MIND READING COMPUTERS

People express their mental states, including emotions, thoughts, and desires, all the time through facial expressions, vocal nuances and gestures. This is true even when they are interacting with machines. Our mental states shape the decisions that we make, govern how we communicate with others, and affect our performance. The ability to attribute mental states to others from their behavior and to use that knowledge to guide our own actions and predict those of others is known as theory of mind or mind-reading.

Existing human-computer interfaces are mind-blind — oblivious to the user's mental states and intentions. A computer may wait indefinitely for input from a user who is no longer there, or decide to do irrelevant tasks while a user is frantically working towards an imminent deadline. As a result, existing computer technologies often frustrate the user, have little persuasive power and cannot initiate interactions with the user. Even if they do take the initiative, like the now retired Microsoft Paperclip, they are often misguided and irrelevant, and simply frustrate the user. With the increasing complexity of computer technologies and the ubiquity of mobile and wearable devices, there is a need for machines that are aware of the user's mental state and that adaptively respond to these mental states.

What is mind reading?

A computational model of mind-reading Drawing inspiration from psychology, computer vision and machine learning, the team in the Computer Laboratory at the University of Cambridge has developed mind-reading machines — computers that implement a computational model of mind-reading to infer mental states of people from their facial signals. The goal is to enhance human-computer interaction through empathic responses, to improve the productivity of the user and to enable applications to initiate interactions with and on behalf of the user, without waiting for explicit input from that user. There are difficult challenges:

Using a digital video camera, the mind-reading computer system analyzes a person's facial expressions in real time and infers that person's underlying mental state, such as whether he or she is agreeing or disagreeing, interested or bored, thinking or confused.

Prior knowledge of how particular mental states are expressed in the face is combined with analysis of facial expressions and head gestures occurring in real time. The model represents these at different granularities, starting with face and head movements and building those in time and in space to form a clearer model of what mental state is being represented. Software from Nevenvision identifies 24 feature points on the face and tracks them in real time. Movement, shape and colour are then analyzed to identify gestures like a smile or eyebrows being raised. Combinations of these occurring over time indicate mental states.

For example, a combination of a head nod, with a smile and eyebrows raised might mean interest. The relationship between observable head and facial displays and the corresponding hidden mental states over time is modeled using Dynamic Bayesian Networks.

Why mind reading?

The mind-reading computer system presents information about your mental state as easily as a keyboard and mouse present text and commands. Imagine a future where we are surrounded with mobile phones, cars and online services that can read our minds and react to our moods. How would that change our use of technology and our lives? We are working with a major car manufacturer to implement this system in cars to detect driver mental states such as drowsiness, distraction and anger.

Current projects in Cambridge are considering further inputs such as body posture and gestures to improve the inference. We can then use the same models to control the animation of cartoon avatars. We are also looking at the use of mind-reading to support on-line shopping and learning systems.

The mind-reading computer system may also be used to monitor and suggest improvements in human-human interaction. The Affective Computing Group at the MIT Media Laboratory is developing an emotional-social intelligence prosthesis that explores new technologies to augment and improve people's social interactions and communication skills.

How does it work?

The mind reading actually involves measuring the volume and oxygen level of the blood around the subject's brain, using technology called functional near-infrared spectroscopy (fNIRS).

The user wears a sort of futuristic headband that sends light in that spectrum into the tissues of the head where it is absorbed by active, blood-filled tissues. The headband then measures how much light was not absorbed, letting the computer gauge the metabolic demands that the brain is making.

The subjects were then asked to rate the difficulty of the tasks, and their ratings agreed with the work intensity detected by the fNIRS system up to 83 ."We don't know how specific we can

be about identifying users' different emotional states," cautioned Sergio Fantini, a biomedical engineering professor at Tufts. "However, the particular area of the brain where the blood-flow change occurs should provide indications of the brain's metabolic changes and by extension workload, which could be a proxy for emotions like frustration."

"Measuring mental workload, frustration and distraction is typically limited to qualitatively observing computer users or to administering surveys after completion of a task, potentially missing valuable insight into the users' changing experiences.

A computer program which can read silently spoken words by analyzing nerve signals in our mouths and throats, has been developed by NASA.

Mind reading computer may be defined as a machine that infers the human being's mental states. The understanding of a human's thoughts is one of the most complex tasks. No one knows what a person would do in the upcoming second by executing his present thoughts or what would a person thought about any other person or what would a person desires and many more. But a mind reading computer could give answer to all these questions. Mind reading computer infers the thoughts of a human being based on various technologies for example by scanning the facial expressions along with head gestures and by identifying the volume and oxygen level inside the blood which is flowing in the vicinity of the brain. With exponential development in the technologies we can say that in future we might have number of technologies that will lead into making the flawless mind reading computer. The ability of mind reading by a computer can provides us many applications in the field of medical, crime and one's life also.

MIND READING &NECESSITY OF MIND READING

Mind reading may be defined as the inferring of the human thoughts, emotions and desires etc. First simplest step of mind reading is by simply understanding the facial expression given by the person as people express their mental states mostly through facial expressions and gestures. No matter whether they are interacting or not. Our mental states shape the decisions that we make, make us react the way we react in a particular situation and thus affect our performance. All over our thoughts are the causes of all the things that are happening. Imagine what happened if we have a computer that can reads mind and after predicting the mental states , if there is any wrong intention possess by any person we can prevent it. And what happened if a wrong intention can be changed into good one by a computer. A computer that can reads and moulds the emotions into the required one, especially in case of a criminal; here no need for a stringent punishment rather a computer is required that can change the mind and hence make the better world than it is now. However, this technology by computer, to change the mind according to a desire is not established now. But in future it might be developed some day. So for all this Design by

MIND READING COMPUTER

The team member of University of Cambridge had been working on a model of mind reading in a computer laboratory and has developed mind reading machines that implement a computational model of mind reading to infer mental states of human being from their facial expressions and head gestures.

This paper describe mind reading computer that infers mental states from facial expressions along with head gestures in real time video. The mental state is recognized by comparing the present real time video with the preinstalled videos which contain different expressions for different mental state (represented by various actions).

Design by

V.Nagarjuna