SRI VENKATESWARA COLLEGE OF ENGINEERING
(Autonomous)
Karakambadi Road, Opposite LIC Training Centre, Tirupati – 517 507.
Accredited by NBA (B.Tech – CSE, ECE and EEE) & NAAC with 'A' Grade
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Department of Electronics and Communication Engineering

FLIPPED CLASSROOM SAMPLE LECTURE NOTES

Class & Subject: **II B.Tech-I Sem & Electronic Circuit Analysis and Design**

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Common Emitter AC Amplifier Design

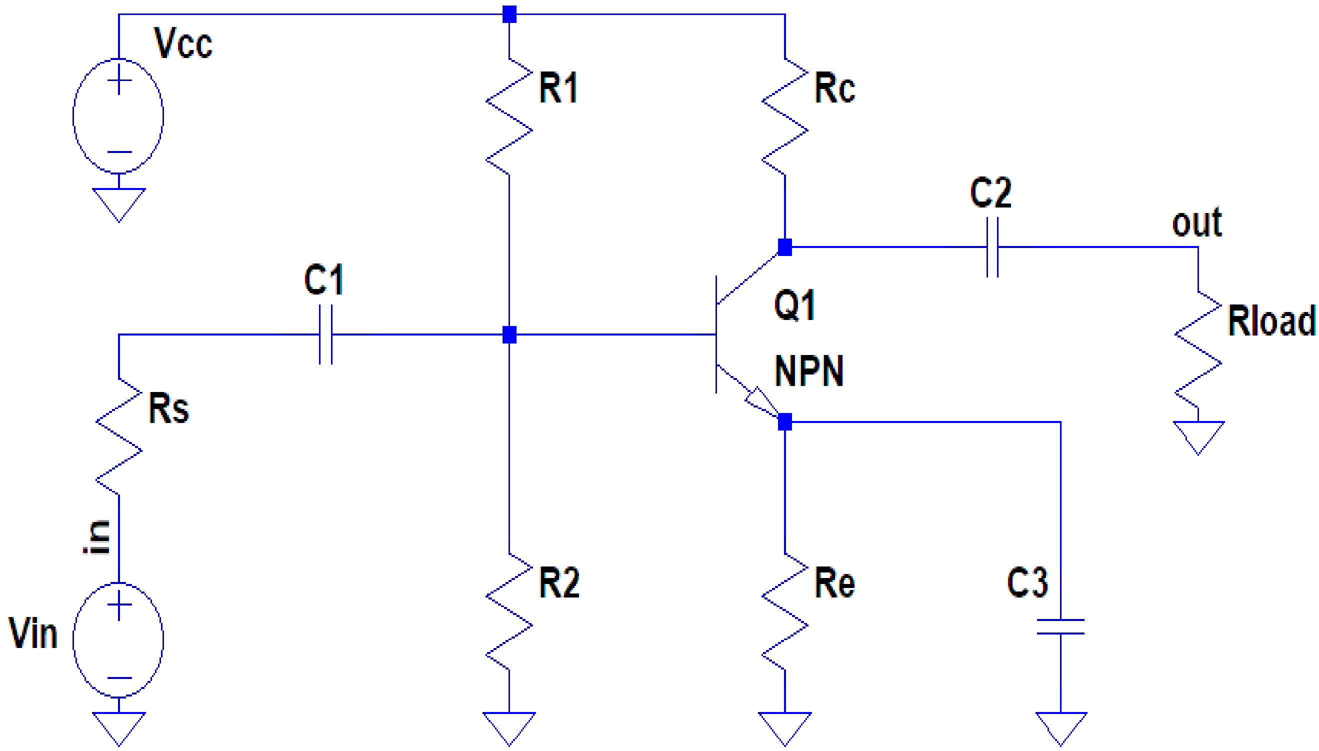
Outcome:

After the class, the student will be able to

1. **Outline** the important steps in carrying out DC analysis and AC analysis of an amplifier circuit.
2. **Design** a Common Emitter AC amplifier for a give set of specifications.
3. **Simulate** the designed circuit and evaluate the parameters.
4. **Justify** the reasons for variations in simulated values with designed values.

Tool used: LTSpice software

The schematic of the Common Emitter AC amplifier is shown below:

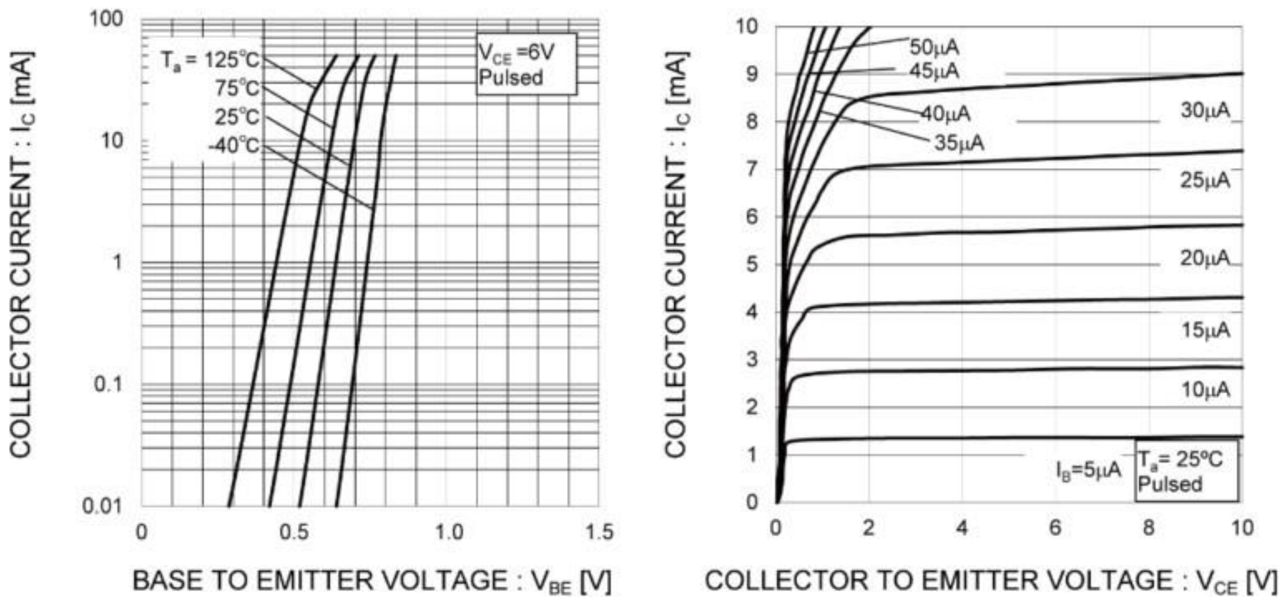


Specifications:

$$f = 1kHz,\ V_{in} = \pm 100mV,\ V_{out} = \pm 5v,\ R_L = 33k, R_{source} = 1k$$

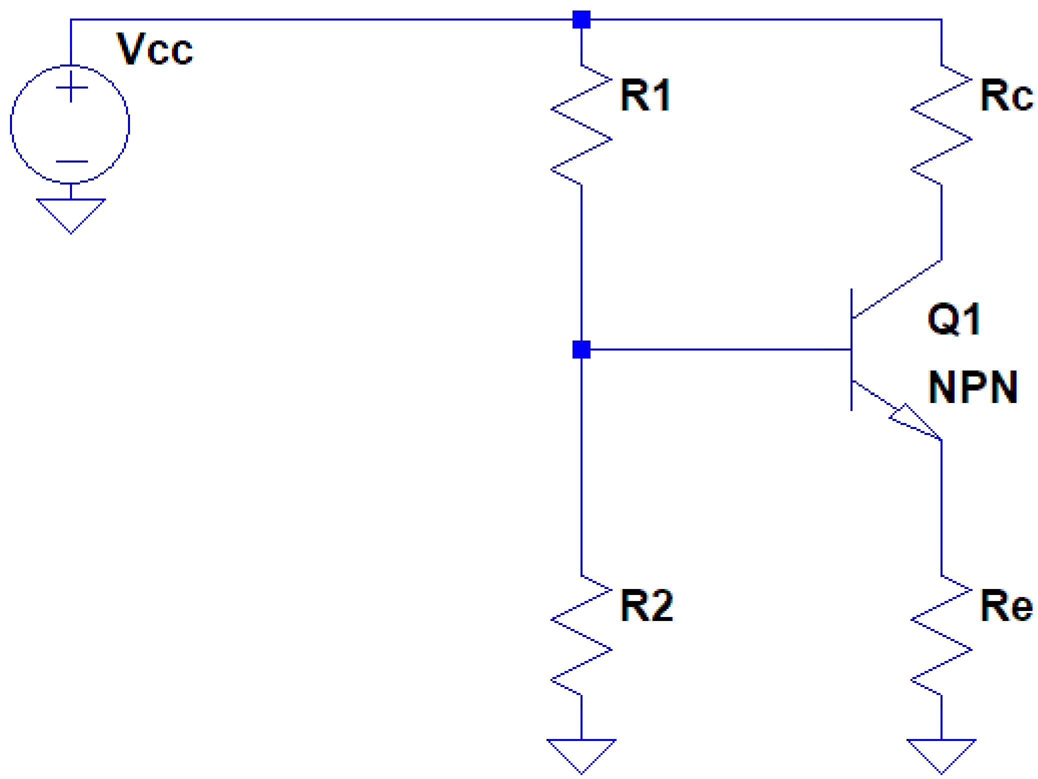
Transistor Selection:

Let us pick a transistor that has good datasheet and good pre-installed model in LTspice. Options are limited. Choose 2SC4102 from the transistor database. The base-emitter voltage and output characteristics shown below are important and give enough information to design.



DC Bias:

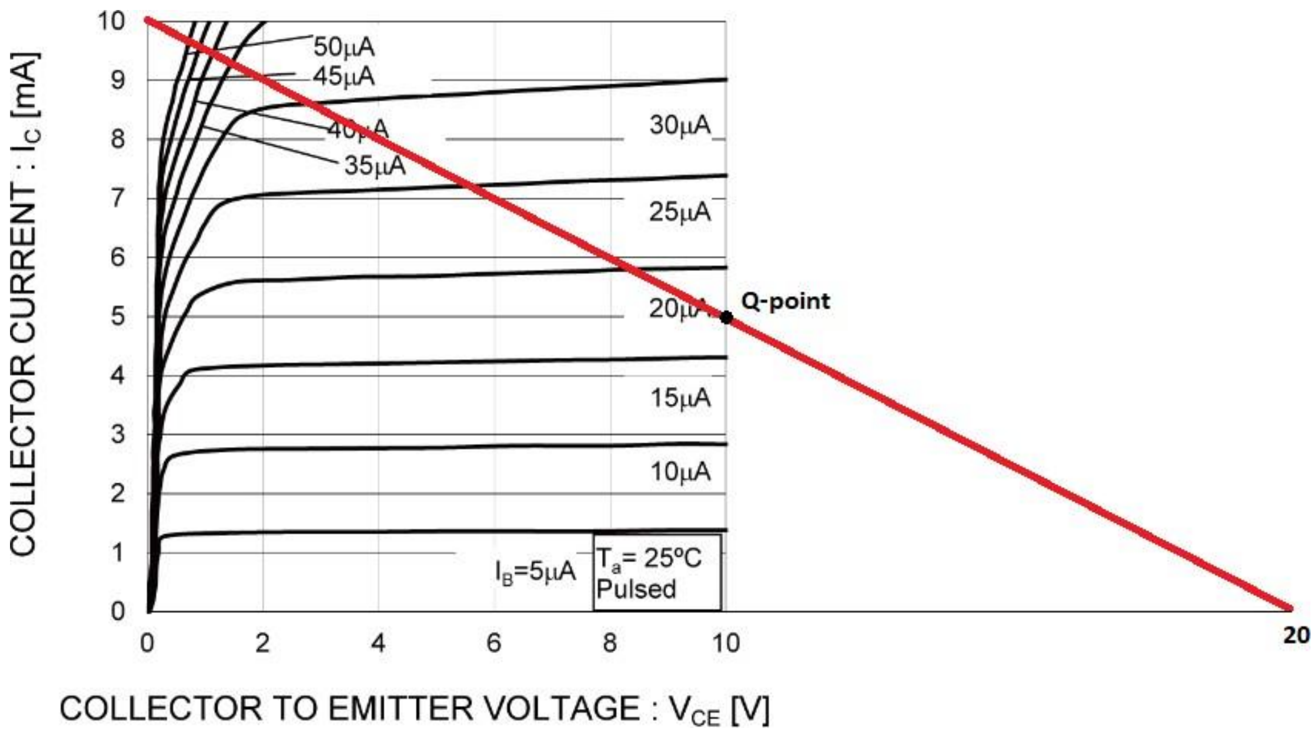
The amplifier design requires the transistor to be in its active region even when no input signal is provided. We need to replace all capacitors with open-circuit (because of the fact that capacitors do not allow DC currents) and eliminate the unnecessary parts to have the following.



Every circuit needs a supply. Let us choose V_{CC}=20V for this one. Secondly, we can choose the collector-emitter voltage and quiescent collector-current looking at the below figure. We are free to choose any point on the figure arbitrarily depending on the application, just like the following.

$$V_{CE(\max)} = V_{CC} = 20V, \qquad V_{CEQ} \triangleq \frac{V_{CE(\max)}}{2} = 10V$$

$$I_{C(max)} = 10mA, \qquad I_{CQ} \triangleq \frac{I_{C(max)}}{2} = 5mA, \qquad I_{BQ} = 17uA$$



Looking at the curves, we can approximate the transistor's gain parameter 'β' for our desired operating-point of I_{CQ}=5mA and V_{CEQ}=10V. Then we can choose the voltages of collector and emitter on quiescent.

$$\beta \cong \frac{5mA}{17uA} \cong 300, \qquad where\ V_{CE} = 10V$$

$$V_{EQ} \triangleq 2.5V, \qquad V_{CQ} \triangleq 12.5V$$

From the graph, V_{BEQ} base-emitter voltage at Q-point

$$V_{BEQ} \cong 0.65V\ @\ I_C = 5mA$$

Now we can calculate the values of biasing resistors R_1 and R_2. As a rule of thumb, we can choose R_1 current as 10 times the base current and R_2 current as 9 times. (Note: for high speed applications, we need to think again)

$$I_{R_1} = 10 I_B = 170uA,$$

$$R_1 = \frac{V_{CC} - (V_{EQ} + V_{BEQ})}{I_{R_1}} \cong 100k,$$

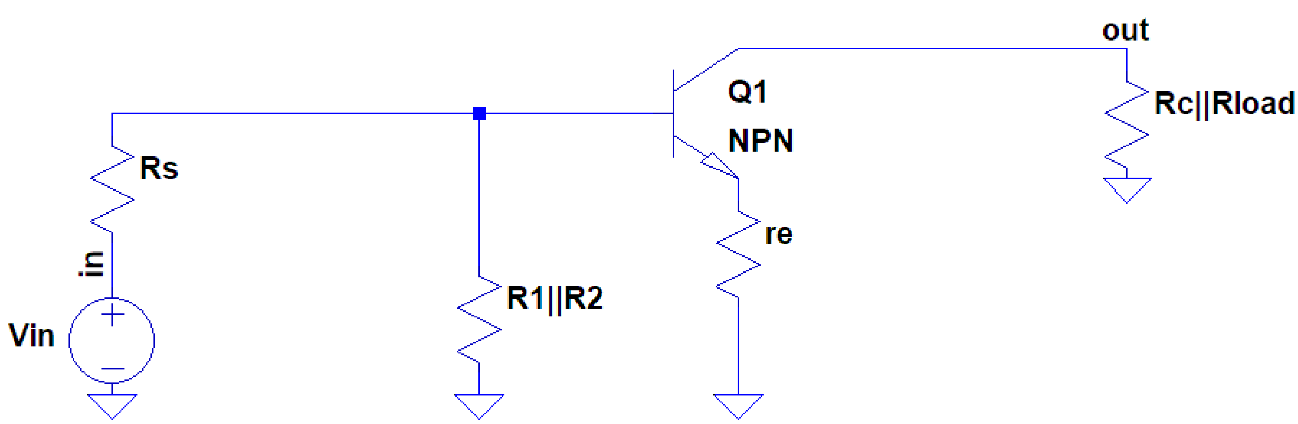
$$R_2 = \frac{V_{EQ} + V_{BEQ}}{I_{R_1} - I_{BQ}} \cong 22k$$

$$R_C = \frac{V_{CC} - V_{CQ}}{I_{CQ}} = 1.5k,$$

$$R_E = \frac{V_{EQ}}{I_{EQ}} = \frac{V_{EQ}}{I_{CQ} + I_{BQ}} \cong 470\,\text{ohm}$$

AC Analysis

Now replace all DC voltage sources and capacitors with short-circuits (because we will choose capacitor values such that they pass the designed AC input frequency with little attenuation). So the AC model is drawn as shown below

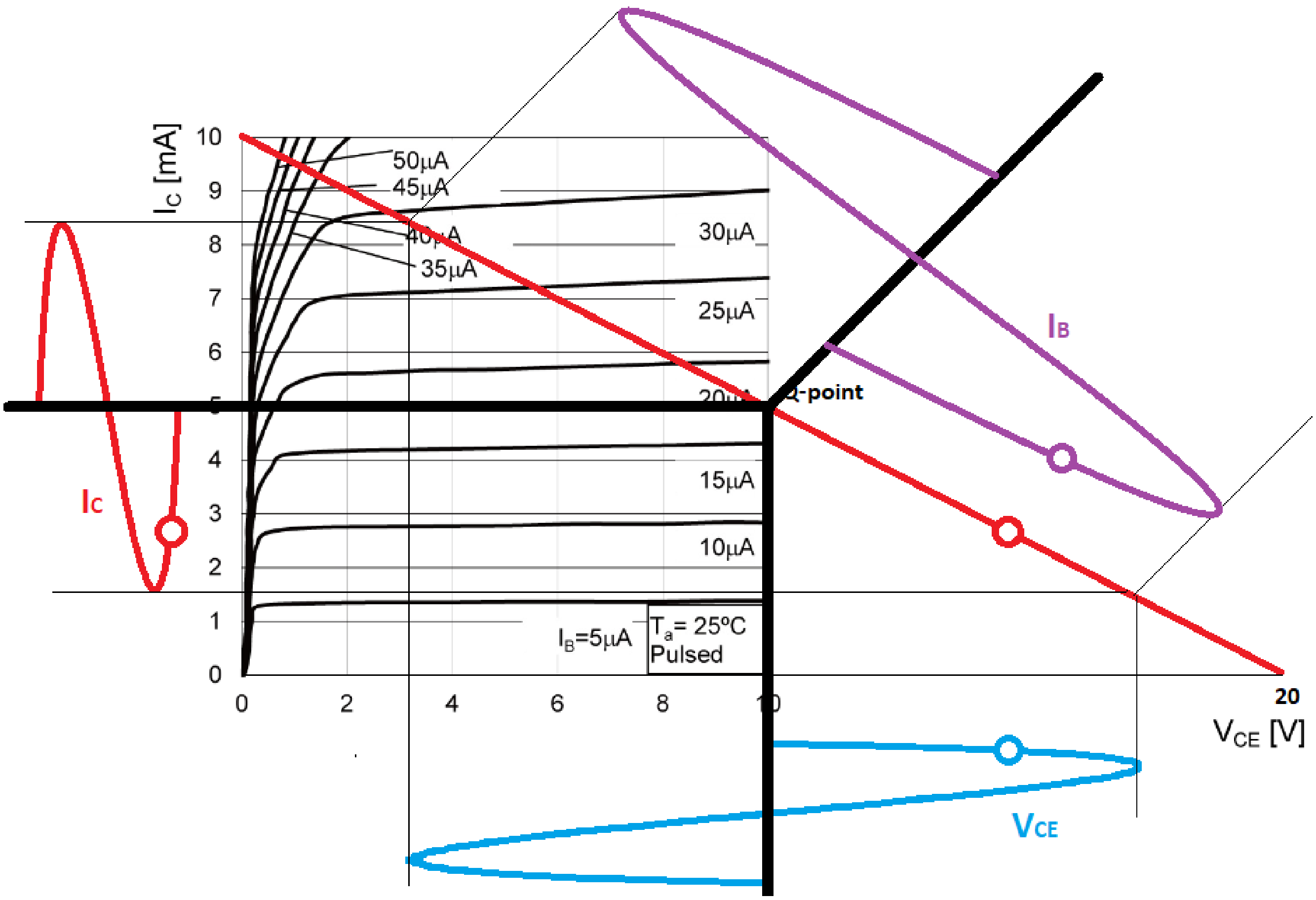


Calculate the peak-to-peak output and base currents using R_{out} , the equivalent output resistance.

$$R_{out} = R_C || R_L \cong 1.435k, \ I_{C(PP)} = \frac{V_{out}}{R_{out}} \cong \pm 3.5mA,$$

$$I_{B(PP)} = \frac{I_{C(PP)}}{\beta} \cong \pm 12uA$$

AC operation is illustrated in the following graph. When base current changes, collector current and collector-emitter voltage change respectively. It is visible that while base current and collector current increases, collector-emitter voltage decreases to cause 180* phase difference between input and output.



Note that the transistor has an intrinsic emitter resistance that is labeled as r_e in the AC equivalent circuit and its approximate value depends on the thermal voltage V_T (approximately 26mV@25*C) and quiescent emitter-current I_{EQ}. The resistance that is seen from base is β-times and input resistance depends on its value.

$$r_E = \frac{V_T}{I_{EQ}} = 5.18\,\text{Ohm}$$

$$r_B = \beta r_E \cong 1.5k,\ R_{in} = R_1||R_2||r_B = 1.38k$$

A: $V_{r_B} = r_B I_{B(PP)} = 17mV, \quad R_s = \frac{V_{in} - V_{r_B}}{V_{r_B}/R_{in}} - R_{source} \cong 5.6k$

Theoretical gain depends only on output resistance and intrinsic emitter resistance of the designed amplifier while the overall gain is affected also by the source resistance.

$$A_{int} = -\frac{R_{out}}{r_E} = 277,$$

$$A = \frac{V_{out}}{V_{in}} = A_{int}\frac{R_{in}}{R_s + R_{source} + R_{in}} = -48$$

AC Coupling Capacitors:

The coupling capacitors have to bypass DC biasing successfully. That is why they should be selected to have less than 1% capacitive-reactance XC than the equivalent resistances they bypass.

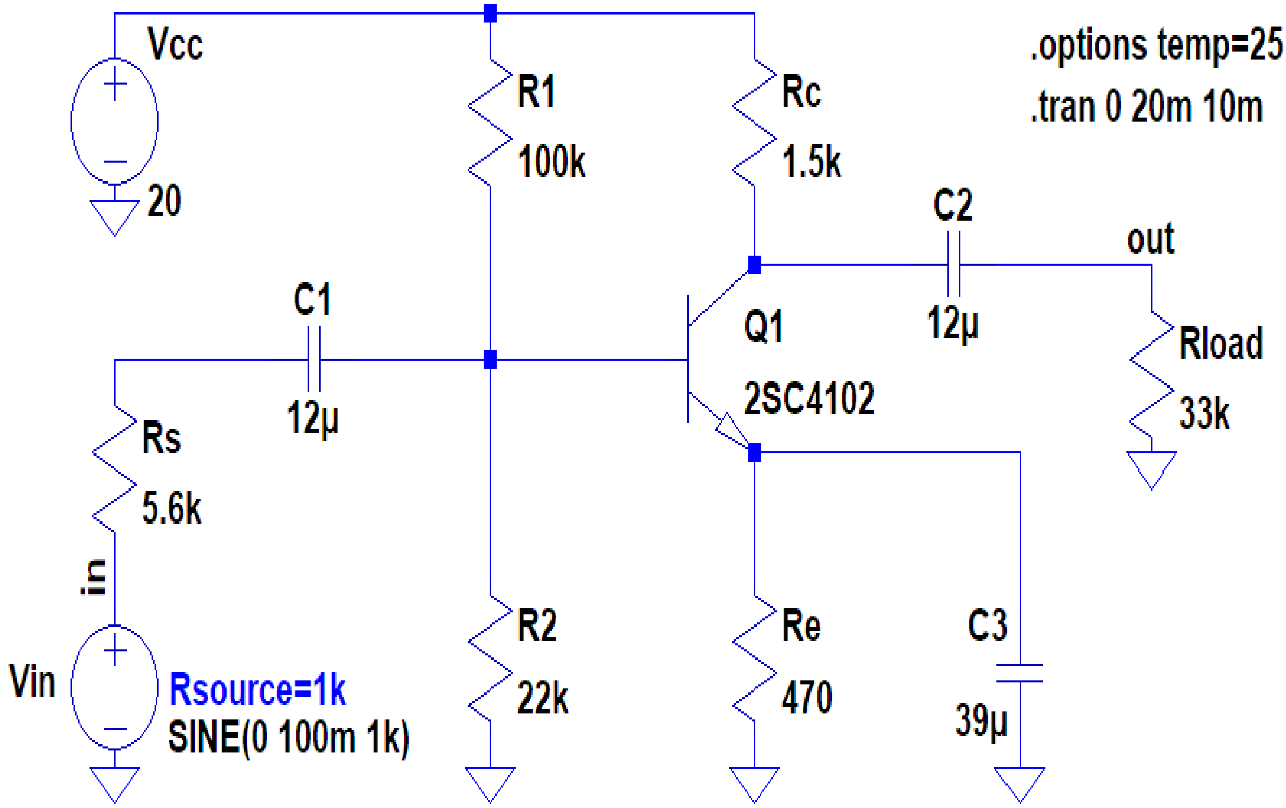
$$X_{C1} = \frac{1}{2\pi f C_1}, \qquad C_1 > \frac{1}{2\pi f(0.01R_{in})} = 11.5uF, \qquad C_1 \triangleq 12uF$$

$$X_{C2} = \frac{1}{2\pi f C_2}, \qquad C_2 > \frac{1}{2\pi f(0.01R_{out})} = 11uF, \qquad C_2 \triangleq 12uF$$

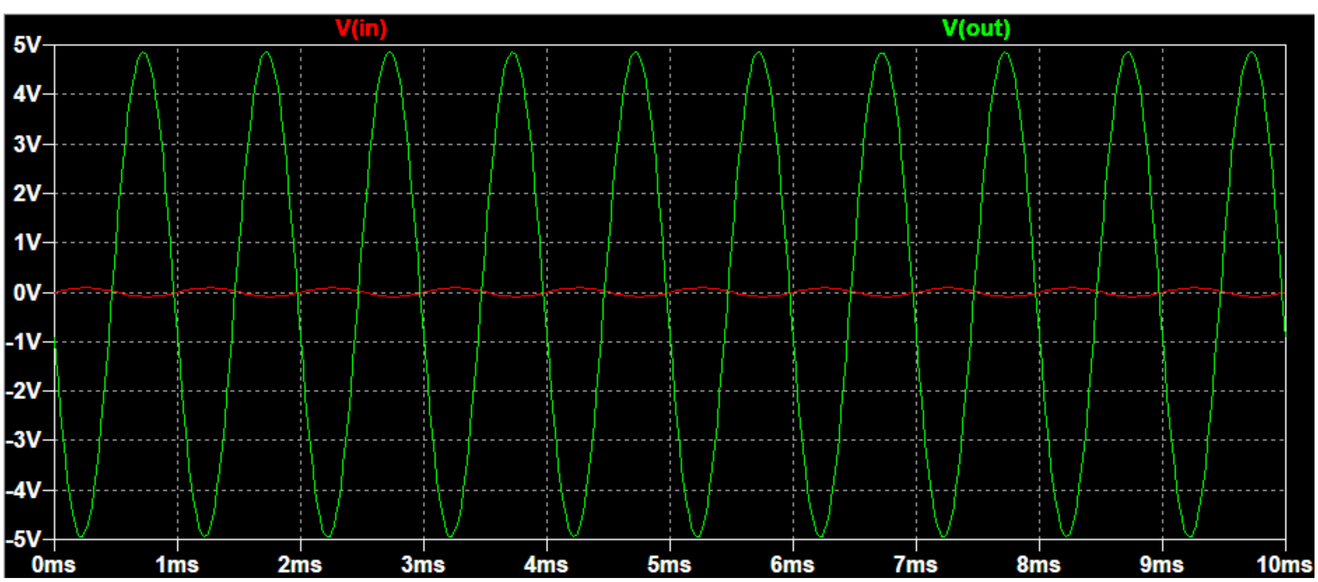
$$X_{C3} = \frac{1}{2\pi f C_3}, \qquad C_3 > \frac{1}{2\pi f(0.01R_E)} = 34uF, \qquad C_3 \triangleq 39uF$$

Simulation and Verification:

The amplifier circuit is simulated using LTspice simulation software and note that **T_A is set to 25°C.**

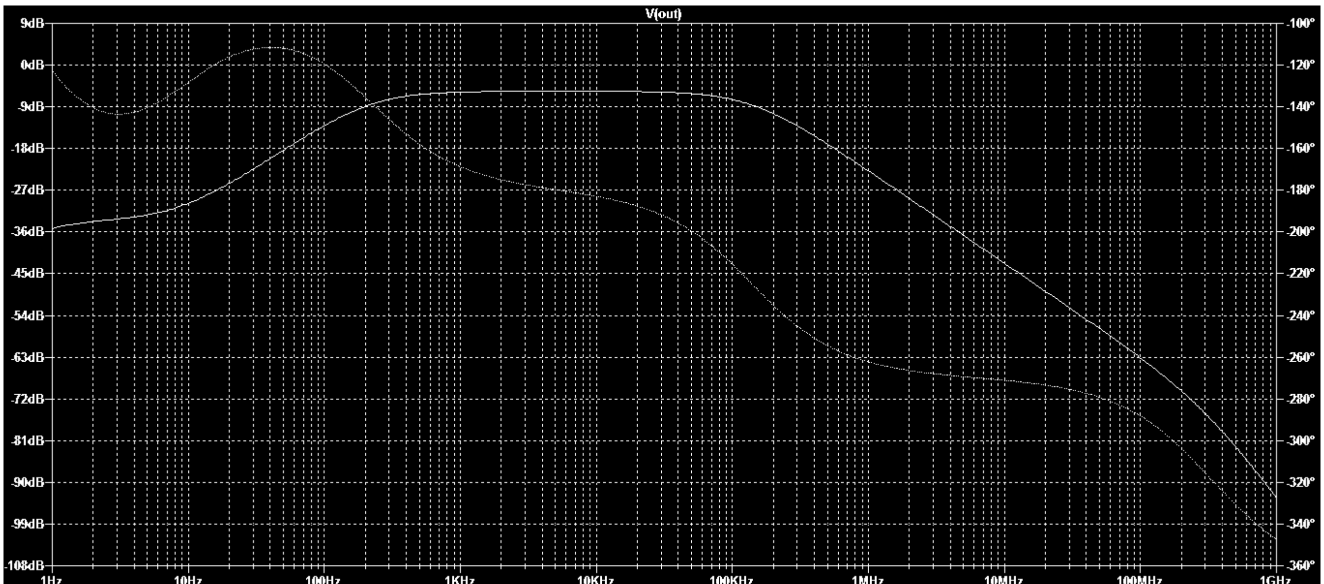


The Transient response analysis is given by



Output amplitude is ±4.9V which is very close to the desired output of ±5V and gain of -49 is very close to the calculated gain of -48. Reasons for the slight variations in the simulated values are due to the assumptions, approximations and model variations considered.

Simulate the amplifier circuit for AC analysis and calculate Bandwidth and Gainbandwidth product.



Similarly, Simulate the amplifier circuit for Noise analysis.