

**SRI VENKATESWARA
COLLEGE OF ENGINEERING
(AUTONOMOUS)**

Department of Electronics and Communication Engineering



RISE MAGAZINE

**Recent Innovations In Sophisticated
Electronics**





DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

RISE-MAGAZINE

Recent Innovations In Sophisticated Electronics

EDITORIAL BOARD:

- 1 Dr. D Srinivasulu Reddy, HOD
- 2 Dr. T. Kaliraja, Prof.
- 3 Mr. G Naveen Kumar, Asst. Prof.
- 4 22BFA04275- G Muni Vignesh
- 5 23BFA04513- C Vijaya Kumar
- 6 24BFA04049- B Kusuma

STUDENTS:

- 1 23BFA04265- M N Nandini
- 2 23BFA04320- Sreenadh Reddy
- 3 23BFA04087- Kalyani
- 4 24BFA04066- Deepika Sri
- 5 24BFA04131- S Sai Nikitha

INSIDE THIS ISSUE:

- 1 Improving Efficiency of AB-Class Audio Power Amplifier Using Thermoelectric Generators
- 2 Dual-Band Dual-Circularly Polarized Shared-Aperture Phased Array for S-/C-Band Satellite Communications
- 3 Easy and Straightforward FPGA Implementation of Model Predictive Control Using HDL Coder
- 4 Application of Deep Dilated Convolutional Neural Network for Non-Flat Rough Surface
- 5 Multi-Path Precharge for GaN Flying-Capacitor-Multi-Level Totem-Pole PFC



DEPARTMENT PROFILE

- Electronics and Communication Engineering has emerged as the major driving force in the present day Information Technology revolution. It is acting as a bridge between different disciplines of engineering and technology. It has penetrated into other prominent sectors such as health care, instrumentation, agriculture, automation, signal processing, remote sensing etc., The recent developments such as IoT, Artificial Intelligence and the mercurial advancements in the field of communication.

Vision

- To be a focal centre for academic excellence in competing global standards and dynamics in the field of Electronics and Communication Engineering with research and services focusing on effective communication skills, entrepreneurial, ethical and social concern.

Mission

- To impart quality technical education in Electronics and Communication Engineering with well established infrastructure, state of the art laboratories, core instructions and cognizant faculty.
- To prepare the young and dynamic Electronics and Communication Engineers professionally deft and intellectually adept with knowledge, behaviour and information competency.
- To enable the learners for changing trends in the field of Electronics and Communication Engineering with a focus on career guidance, placements and higher education by Industry-Institute relationship.

SV College of Engineering Tirupati
svce.edu.in

PROGRAM EDUCATIONAL OBJECTIVES

PEO1: Graduates should be cognizant in basic science, fundamental engineering stream along with core related domains in ECE and Allied fields.

PEO2: Graduates should understand issues related to design, problem solving, and intellectually adept with knowledge, behavior and information competency.

PEO3: Graduates should demonstrate their technical, communication, research, aptitudes along with leadership skills in professional environment to empower employability, higher education and entrepreneurs successfully through industry-institute interaction.

PEO4: Graduate should be motivated with high ethical, human values and team work towards development of the societ.

PROGRAM OUTCOMES

PO1: ENGINEERING KNOWLEDGE: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: PROBLEM ANALYSIS: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: DESIGN/DEVELOPMENT OF SOLUTIONS: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: CONDUCT INVESTIGATIONS OF COMPLEX PROBLEMS: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: MODERN TOOL USAGE: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: THE ENGINEER AND SOCIETY: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: ENVIRONMENT AND SUSTAINABILITY: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: ETHICS: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: INDIVIDUAL AND TEAM WORK: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: COMMUNICATION: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: PROJECT MANAGEMENT AND FINANCE: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: LIFE-LONG LEARNING: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

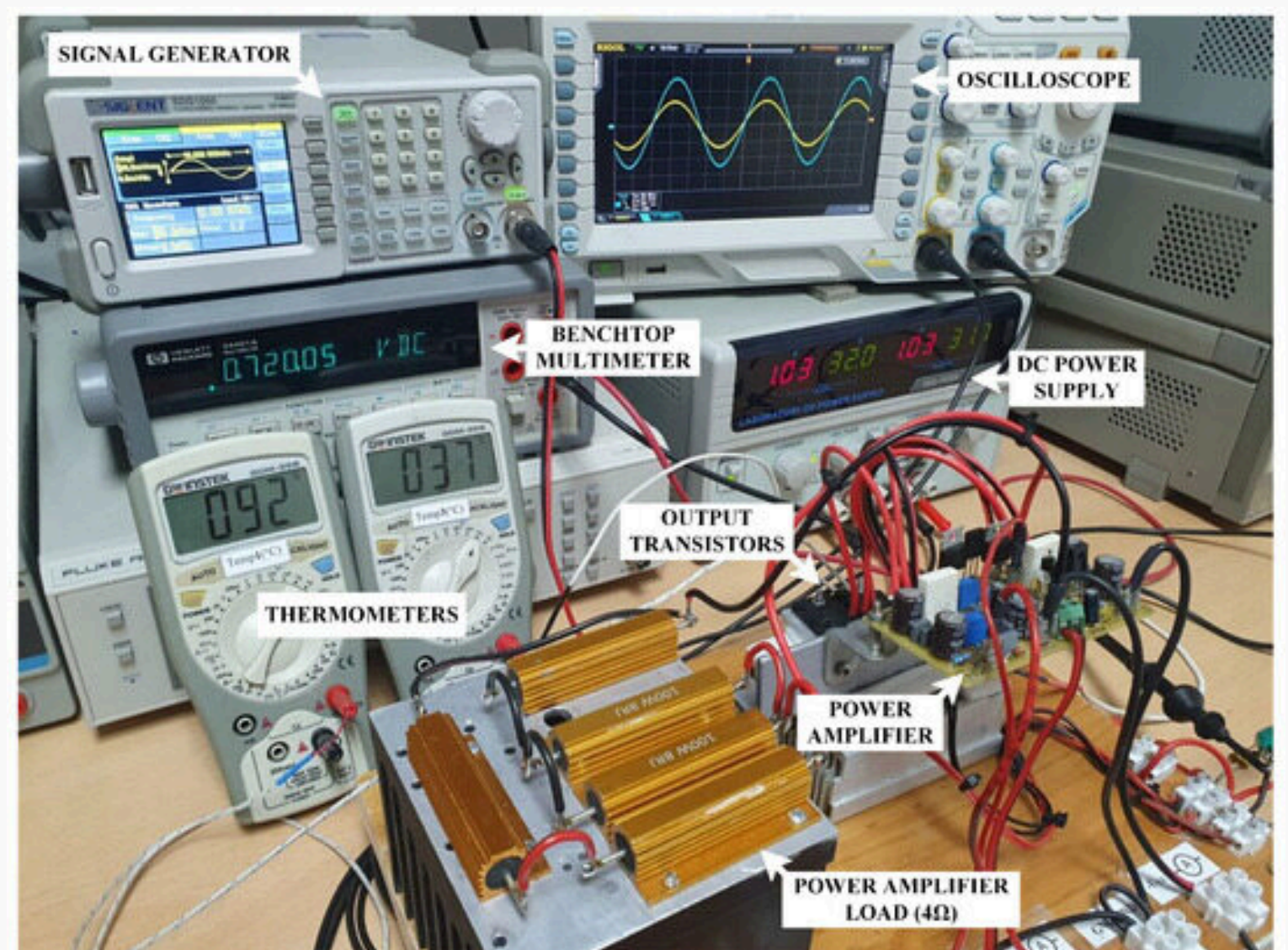
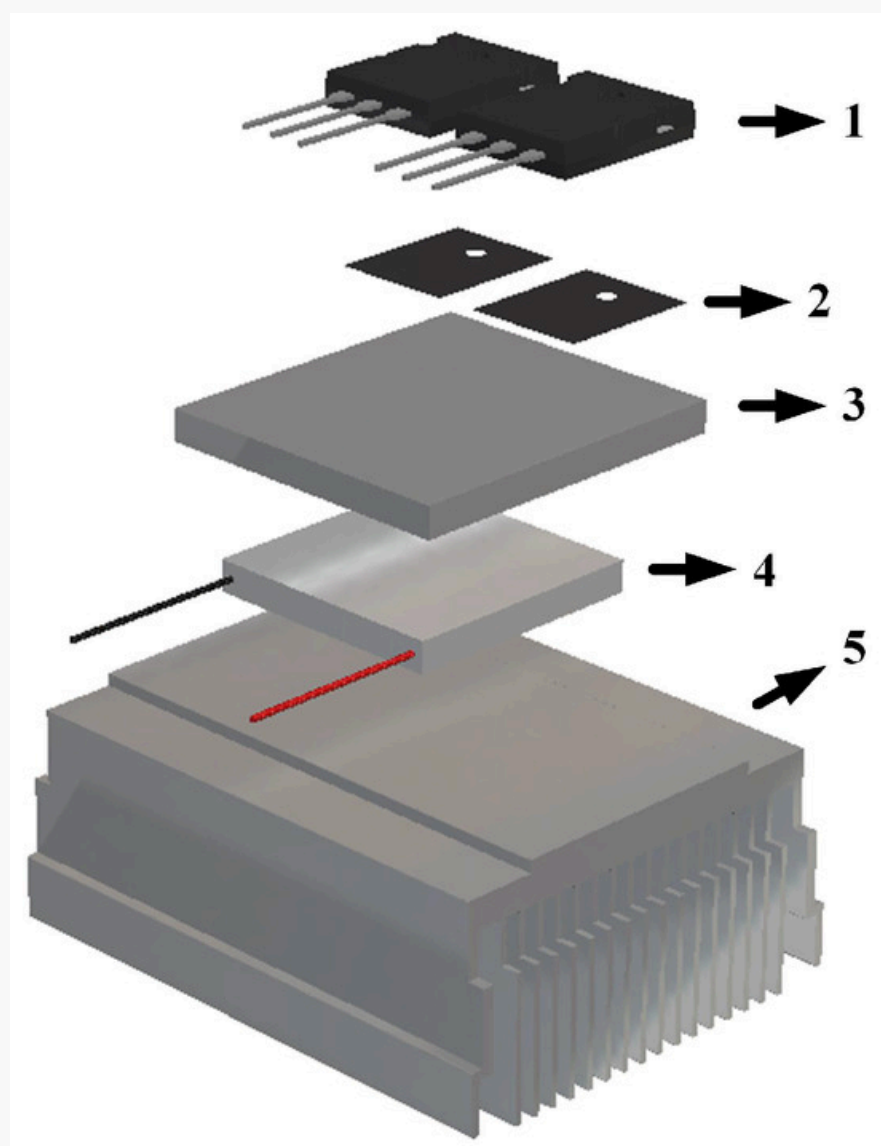
PROGRAM SPECIFIC OUTCOMES

PSO1: An ability to get an employment in Electronics and Communication Engineering field and related industries and to participate & succeed in competitive examinations like GRE, GATE, TOEFL, PSUs, etc.

PSO2: Should be able to design and test various electronic systems that perform analog and digital processing functions.

Improving Efficiency of AB-Class Audio Power Amplifier Using Thermoelectric Generators ----- **23BFA04265- M N Nandini**

Since circuit-based solutions for increasing the efficiency of Class AB audio amplifiers have reached their peak, this article presents a non-circuit-based approach for the same purpose. The output transistors of this class of amplifiers dissipate a significant amount of thermal energy, resulting in relatively low amplifier efficiency and requiring the transistors to be mounted on large heatsinks. This study was conducted with the aim of capturing the waste heat energy dissipated by the output transistors and converting it into electrical energy using thermoelectric generators (TEGs), which can then be used to increase the efficiency of the amplifier system. In addition to improving efficiency, this study aims to determine the extent to which heatsinks with smaller dimensions can be used in combination with the amplifier through the use of TEGs, potentially leading to a wider commercial application of Class AB audio amplifiers. The experimental results show that the thermoelectric conversion efficiency of TEGs reached 1.097% in the best case, indicating a potential increase of 0.275% in the overall efficiency of the amplifier system. These results show that the low thermoelectric efficiency of TEGs is a limiting factor that prevents a breakthrough in improving the efficiency of the power amplifier system with the proposed non-circuit-based approach.



Class AB audio power amplifiers are characterized by higher efficiency compared to Class A and lower linear distortion compared to Class B amplifiers.

Due to the good balance between efficiency and sound reproduction quality, Class AB power amplifiers are still the most commonly used amplifiers in high-performance audio systems.

In commercial use, however, Class D power amplifiers are taking the lead, as their high efficiency means that they dissipate only small amounts of waste heat. As a result, these amplifiers do not require large heatsinks and are therefore much cheaper to manufacture. In terms of sound reproduction quality, Class AB audio amplifiers are superior to Class D amplifiers.

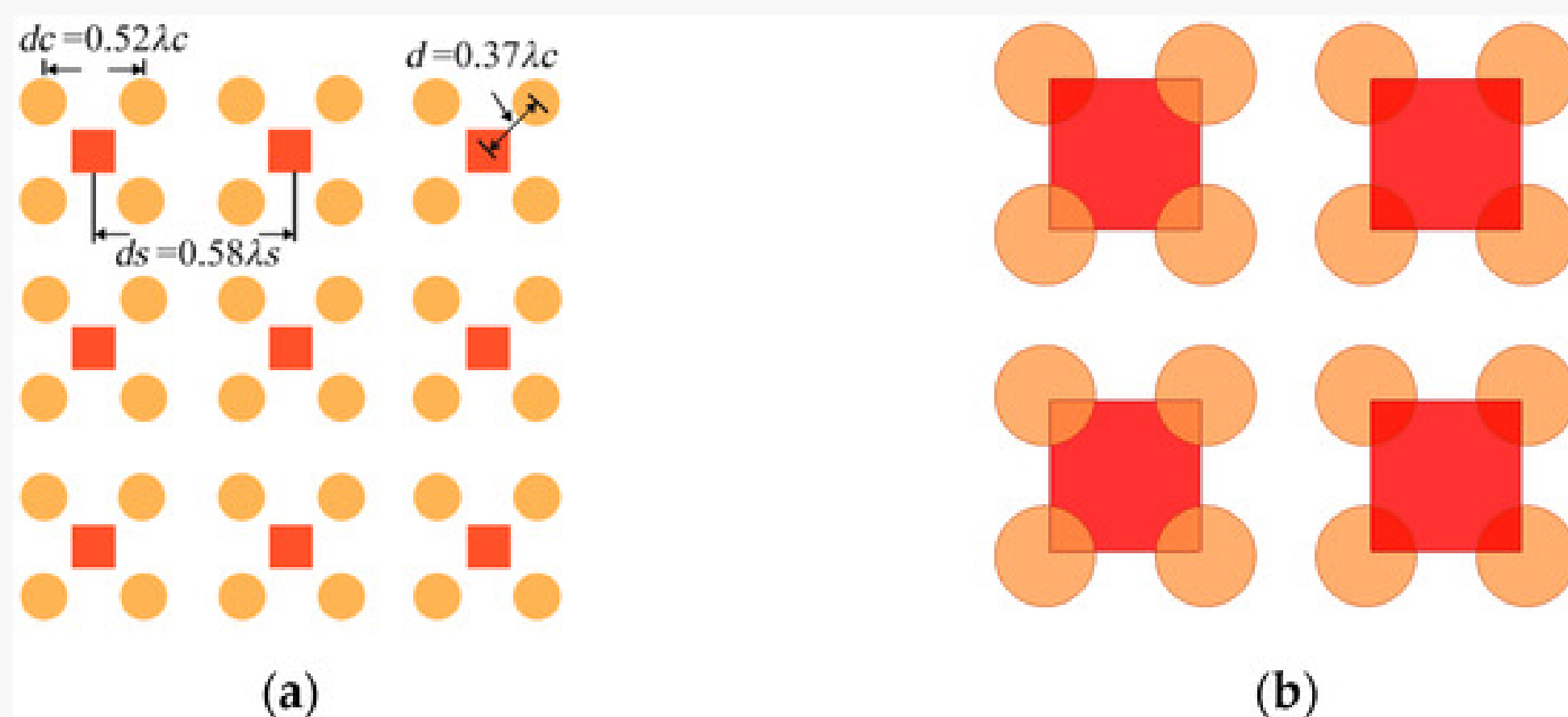
Circuit solutions aimed at increasing the efficiency of Class AB power amplifiers while maintaining high linearity focus on regulating the amplifier's supply voltage as a function of the output signal amplitude. This approach led to the development of Class G and Class H amplifiers.



The wider application of Class AB audio power amplifiers is limited by their relatively low efficiency and the need for large heatsinks. The original assumption that TEGs placed between the output transistors and the heatsink would absorb some of the thermal energy and allow the use of smaller heatsinks in Class AB power amplifiers has not been confirmed. On the contrary, the use of larger heatsinks leads to higher thermoelectric efficiency and higher converted energy. If the converted energy is fed back into the power supply circuit, the efficiency of the system increases only insignificantly. The size of the heatsink used in a Class AB power amplifier system with TEGs must be selected as a compromise between the system temperatures achieved and the amount of energy converted. The low thermoelectric conversion efficiency of TEGs is a limiting factor that prevents the use of smaller heatsinks and a significant improvement in the efficiency of the power amplifier system. This outcome can only be achieved through considerable progress in the development of semiconductor materials for the manufacture of thermocouples, which will lead to a significant increase in the thermoelectric conversion efficiency of TEGs.

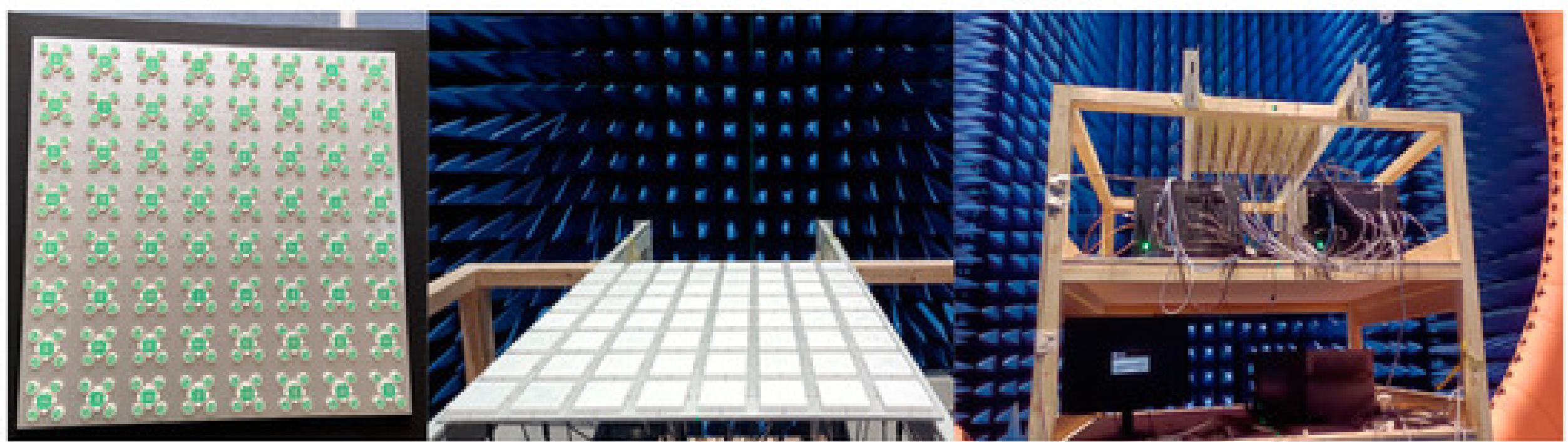
Dual-Band Dual-Circularly Polarized Shared-Aperture Phased Array for S-/C-Band Satellite Communications ----- 23BFA04320- Sreenadh Reddy

In this article, a novel method of achieving a single-layer, dual-band, dual-circularly polarized (CP) shared-aperture phased array antenna with wide beam scanning coverage is presented. The space antenna was designed to provide direct-to-cellular communications services at S-/C-bands with a frequency ratio of 1:1.8. Using novel ceramic substrates with high dielectric constants for antenna miniaturization, the optimum interelement spacing can be ensured in one single layer to meet the large-angle scanning demand. The CP characteristic of the phased array is improved by the sequential rotation technique. A prototype of phased array, which is composed of an 8×8 S-band Rx array and a 16×16 C-band Tx array, is fabricated to verify this design. The measured results show that the shared-aperture phased array can provide $\pm 50^\circ$ beam scanning coverage at both the S- and C-bands simultaneously to meet the direct-to-cellular communication demand in low earth orbit (LEO) satellites.



Commercial off-the-shelf cellular phones, or “stock” cellular phones, have a demand to establish connectivity directly with the satellite for voice, messaging, and basic web browsing services, especially outside the reach of traditional terrestrial mobile networks. Due to the limitation of terrestrial mobile terminals in gain and transmission power, a large aperture of phased array antenna for satellite payload is needed to improve the passive gain and realize direct-to-cellular communications. The space antenna with a large aperture should have the merits of a low-profile, shared aperture for RX/TX, be lightweight, and be deployable to meet the serious demands of limited space, weight, and power in a satellite platform.

This work has selected the S-/C-band for direct-to-cellular communications services, specifically 1.9–2 GHz and 3.4–3.6 GHz for the downlink and uplink, respectively. However, it is costly to support two separate downlink and uplink phase arrays simultaneously, especially for a satellite with limited space and resources. The shared-aperture antenna is thus an attractive candidate due to its compact space and cost-effective manufacture. Circularly polarized (CP) antennas have many advantages over linearly polarized antennas. For example, due to its lower attenuation in complex climatic environments, the CP antenna could penetrate the ionosphere and overcome the Faraday Effect in the ionosphere between satellite and earth communications. Therefore, CP antennas have an important significance in direct-to-cellular communications.

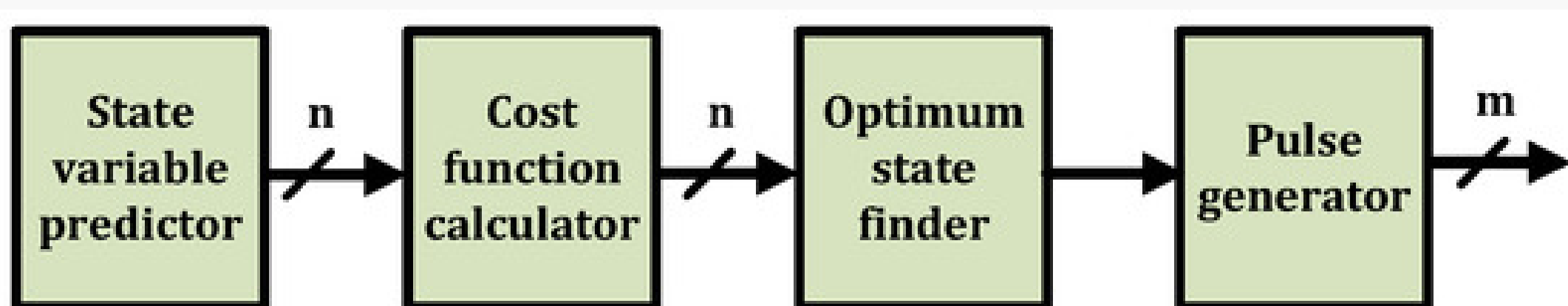


In this paper, a novel S-/C-band RHCP/LHCP shared-aperture phased array with large-angle beam scanning is proposed. The proposed array, based on high-dielectric ceramic technology, is arranged in one single layer. The optimum interelement spacing is ensured by the miniaturization of the elements to provide wide-angle scanning of larger than $\pm 50^\circ$ for both high- and low-frequency bands without a serious grating lobe. The CP characteristic of the phased array is improved by the sequential rotation technique. The simulated and measured results show that the shared-aperture phased array can effectively operate at the S-band (from 1.93 to 2.03 GHz) and C-band (from 3.32 to 3.71 GHz) simultaneously with a large-angle beam scanning up to $\pm 50^\circ$ and a good CP performance with AR less than 3 dB. Furthermore, the as-proposed array is convenient for expanding to a larger aperture phased array for satellite payloads with direct-to-cellular communications capability.

The proposed antenna was simulated and well-optimized according to the required design specifications. This work was simulated and studied through the full-wave simulation software HFSS. Based on the simulated results, the prototype of a dual-band shared-aperture phased array antenna was developed.

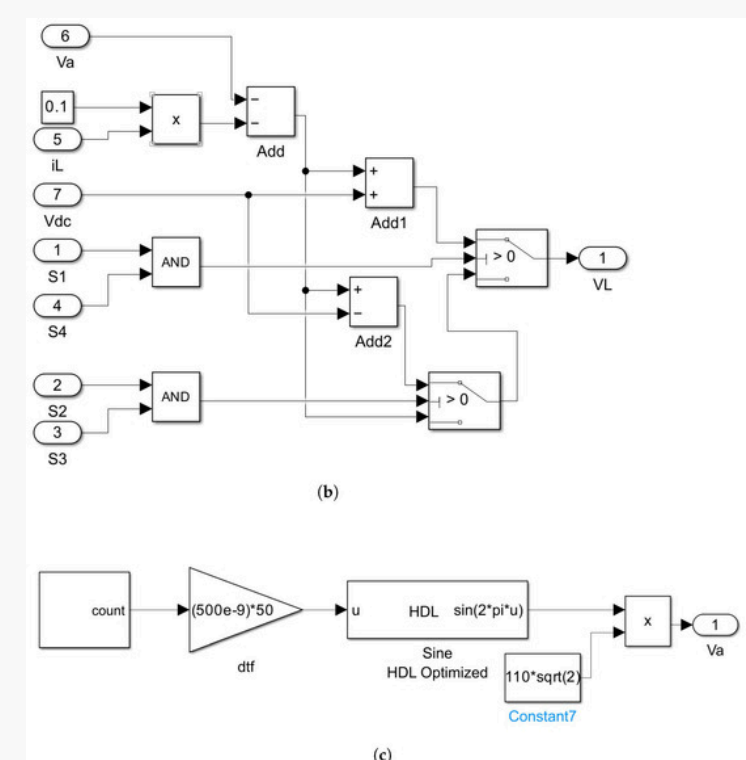
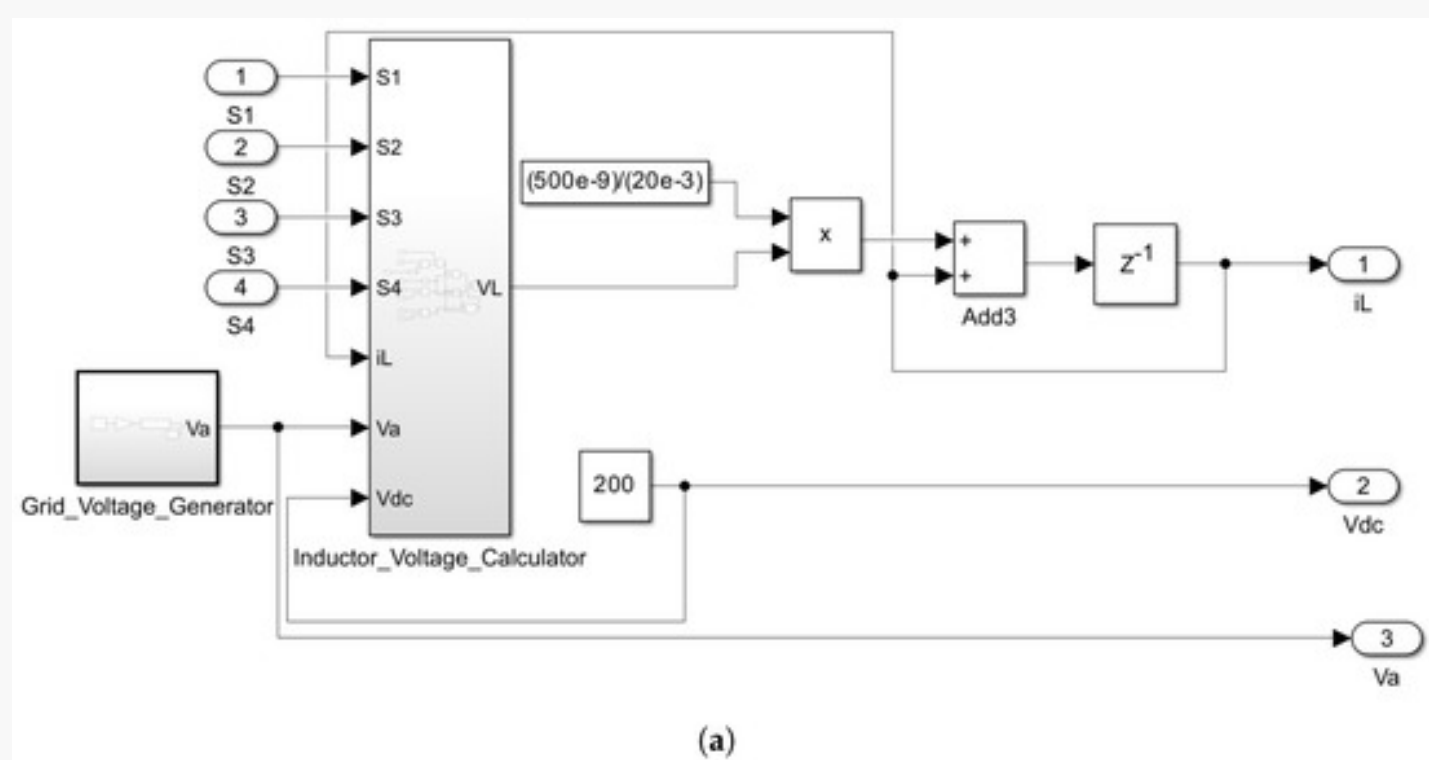
Easy and Straightforward FPGA Implementation of Model Predictive Control Using HDL Coder ----- 23BFA04087- Kalyani

Model Predictive Control (MPC) is widely adopted for power electronics converters due to its ability to optimize system performance under dynamic constraints. However, its FPGA implementation remains challenging due to the complexity of Hardware Description Language (HDL) programming. This paper addresses this challenge by introducing a straightforward methodology that simplifies FPGA implementation using MATLAB R2022b Simulink HDL Coder. It is shown that HDL Coder yields favorable synthesis outcomes, both in terms of area and time, compared to hand-coded HDL. Notably, the proposed method achieves a significantly reduced sampling step for the MPC algorithm down to 32 ns marking a substantial improvement over state-of-the-art implementations. The Integrated Logic Analyzer (ILA) IP available in the Vivado tool is used during the HIL testing phase to facilitate the real-time observation and analysis required for debugging and confirming the FPGA-implemented controller performance. Additionally, this paper discusses the advantages of utilizing HDL Coder for simplifying the FPGA programming process in power electronics applications and addresses the design challenges encountered using this methodology.



Model Predictive Control (MPC) is an advanced control strategy extensively used in power electronics converters, particularly in applications involving DC/AC converters. This approach brings numerous advantages, including its simplicity in design, exceptional dynamic performance, capacity to address multiple control objectives, and simple incorporation of system constraints and nonlinearities. The fundamental parts in MPC algorithms are the prediction model, the cost function, and the optimization algorithm. MPC predicts the system's future behavior within a specified time frame. Subsequently, by computing a cost function, it determines the optimal state to fulfill the controller's objectives. MPC controllers are divided into two main types: Continuous Control Set (CCS) and Finite Control Set (FCS). In CCS-MPC, a fixed frequency can be achieved through the use of a Pulse Width Modulation (PWM) block.

This method involves calculating the control action, such as the modulating signal or duty ratio, and subsequently generating switching pulses. On the other hand, FCS-MPC typically does not aim for a fixed switching frequency. In each step of the control algorithm, FCS-MPCs select the optimal switching state without involving any modulator block. They focus on determining the optimal states from a limited set of switching options available in switching power converters. This flexibility enables the adaptation of choosing the most suitable switching state in each step, resulting in variable switching frequencies rather than maintaining a fixed one. Comparatively, CCS-MPC proves effective for addressing challenges with longer prediction horizons, while FCS-MPC is commonly utilized for applications with shorter prediction horizons in power electronics. Particularly, the FCS-MPC approach has gained notable recognition for its emphasis on reducing the computational burden of the MPC algorithm by acknowledging that power converters can be modeled as discrete systems. However, achieving small sampling steps remains a significant challenge for FCS-MPC implementations, which is addressed in this paper.

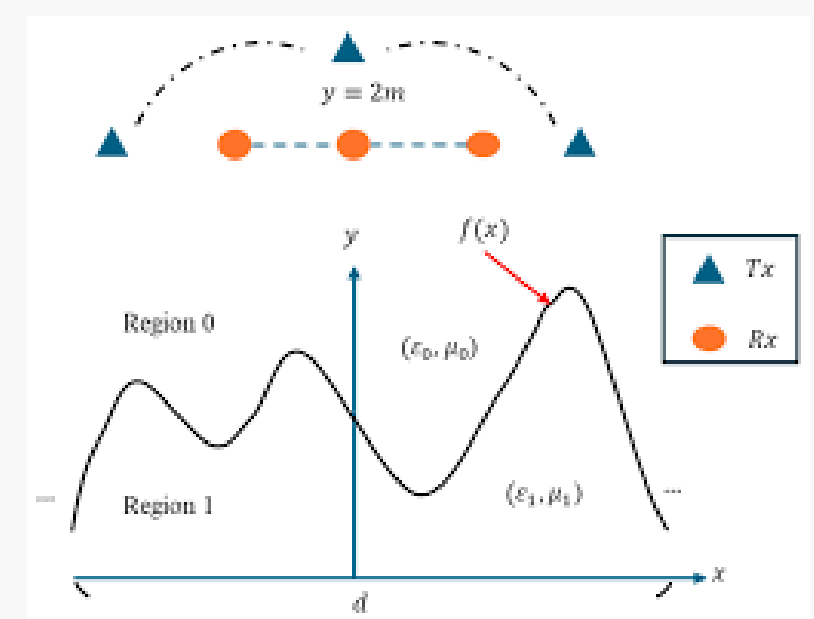
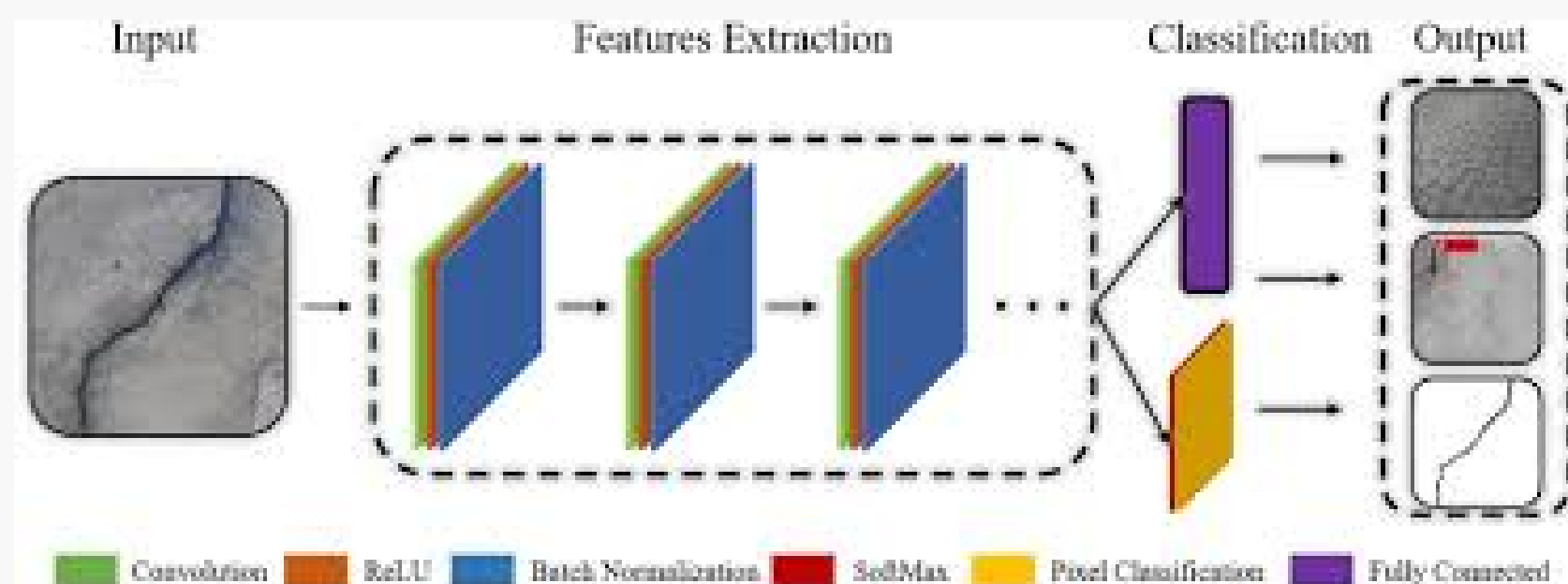


This paper demonstrates the feasibility and practicality of using MATLAB Simulink HDL Coder for FPGA implementation of Model Predictive Control (MPC) algorithms. By applying the methodology to a grid-connected single-phase H-bridge converter, the research highlights the advantages of this approach in simplifying FPGA programming and enabling access to engineers with limited expertise in hardware description languages. A simple case study was intentionally chosen to focus on demonstrating the proposed workflow, rather than the intricacies of the MPC algorithm itself. However, the proposed methodology is adaptable to more complex topologies with minimal changes to the predictive model and cost function, as shown for the three-phase inverter.

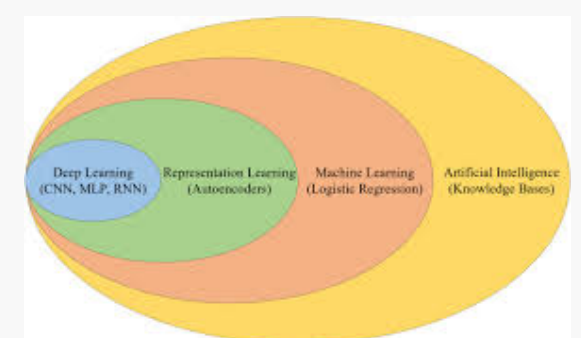
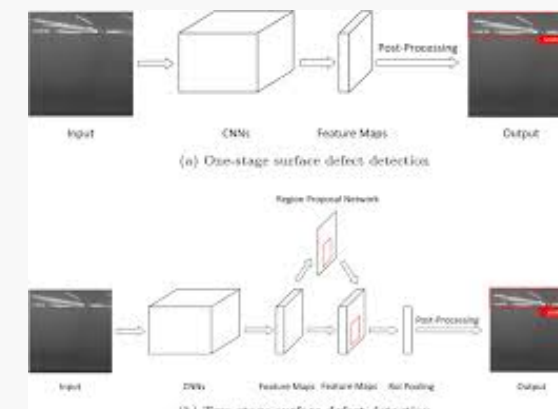
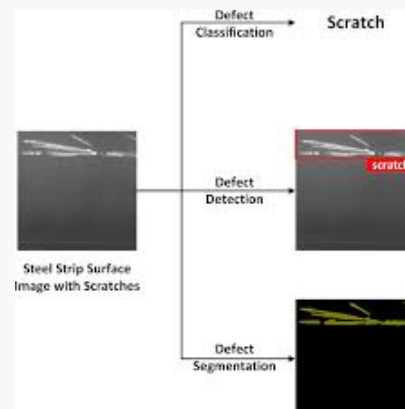
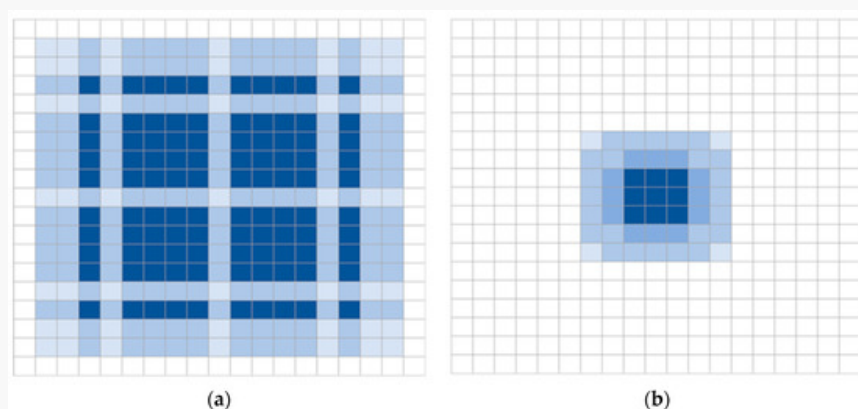
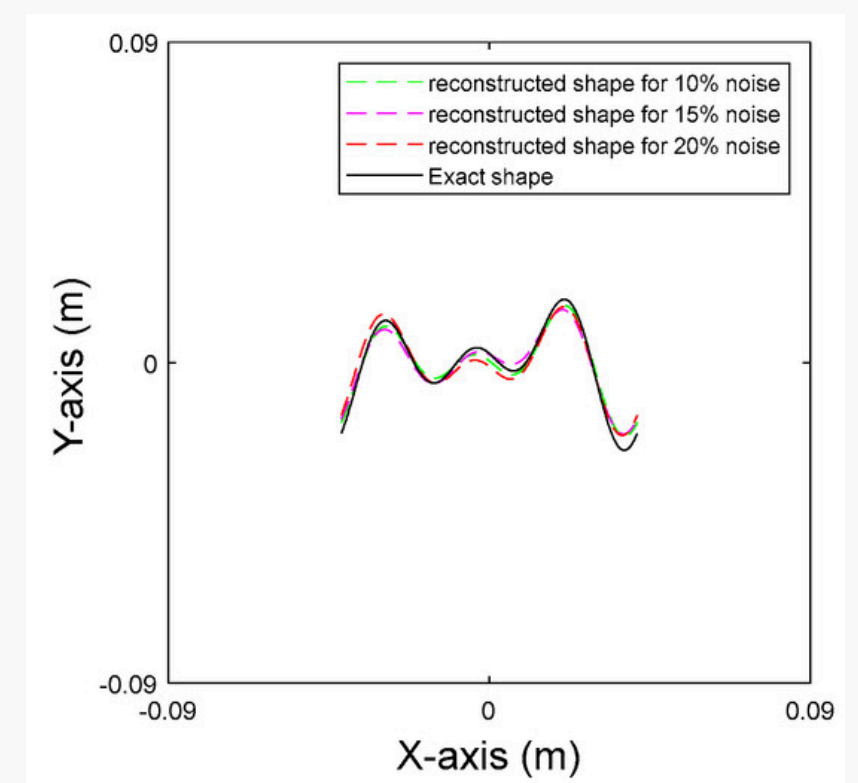
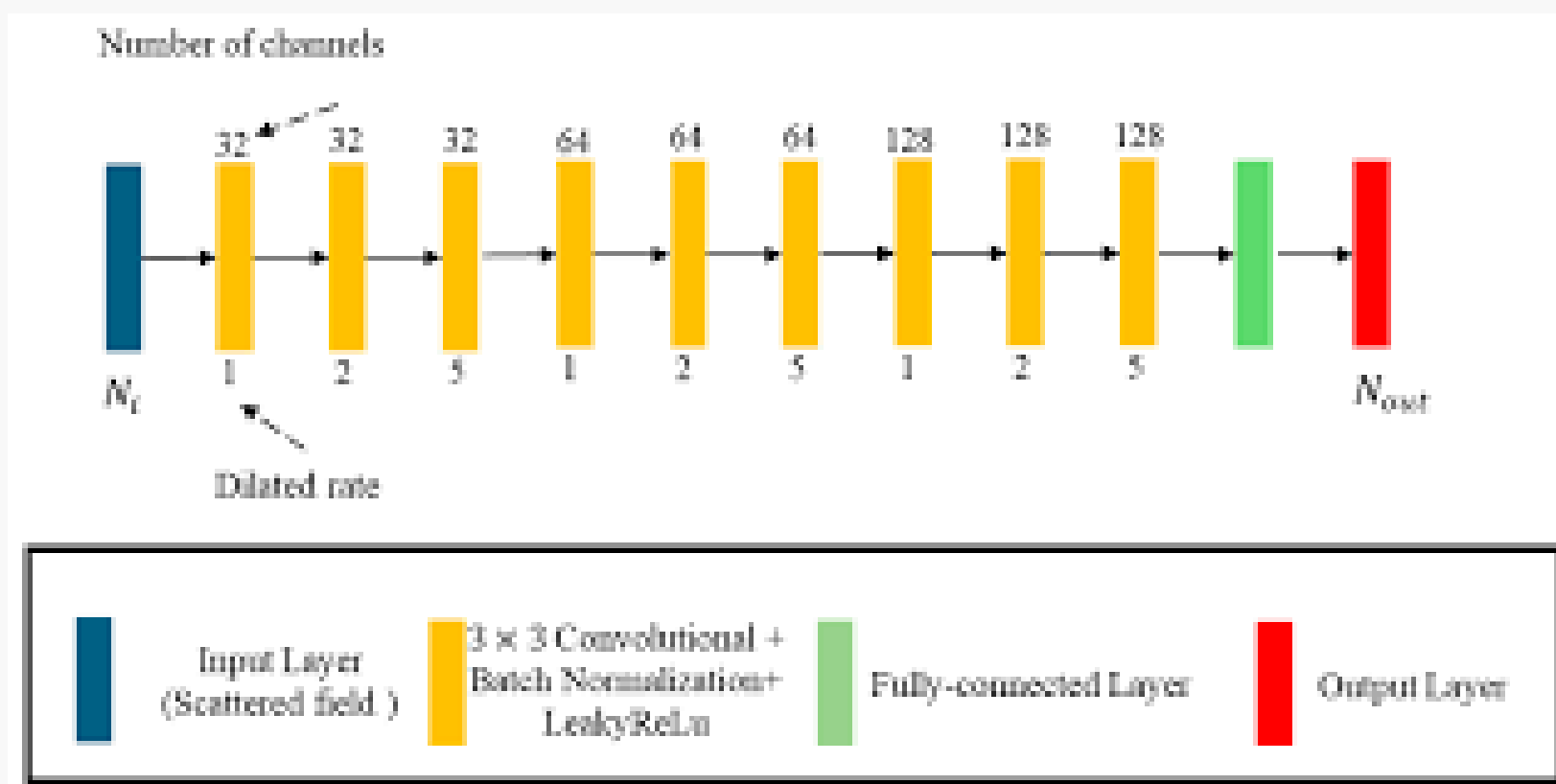
Application of Deep Dilated Convolutional Neural Network for Non-Flat Rough Surface

----- 24BFA04066- Deepika Sri

In this paper, we propose a novel deep dilated convolutional neural network (DDCNN) architecture to reconstruct periodic rough surfaces, including their periodic length, dielectric constant, and shape. Historically, rough surface problems were addressed through optimization algorithms. However, these algorithms are computationally intensive, making the process very time-consuming. To resolve this issue, we provide measured scattered fields as training data for the DDCNN to reconstruct the periodic length, dielectric constant, and shape. The numerical results demonstrate that DDCNN can accurately reconstruct rough surface images under high noise levels. In addition, we also discuss the impacts of the periodic length and dielectric constant of the rough surface on the shape reconstruction. Notably, our method achieves excellent reconstruction results compared to DCNN even when the period and dielectric coefficient are unknown. Finally, it is worth mentioning that the trained network model completes the reconstruction process in less than one second, realizing efficient real-time imaging.



Electromagnetic imaging is an advanced and promising technology that utilizes the emission of electromagnetic waves to illuminate objects within a specified area of interest. By sending these waves into the environment, the system captures the scattered field information that is produced when the electromagnetic waves interact with various materials. These scattered data are subsequently processed to reconstruct crucial details about the object being examined, including its position, shape, and material composition. This innovative imaging technique is increasingly applied across a diverse range of fields. For instance, in surface inspection, it aids in identifying flaws or irregularities in industrial components. In biomedical imaging, it provides insights into the internal structures of biological tissues, enabling better diagnostics and treatment planning. Similarly, in non-destructive testing, it allows the evaluation of materials without causing any harm, ensuring integrity and safety in various applications.

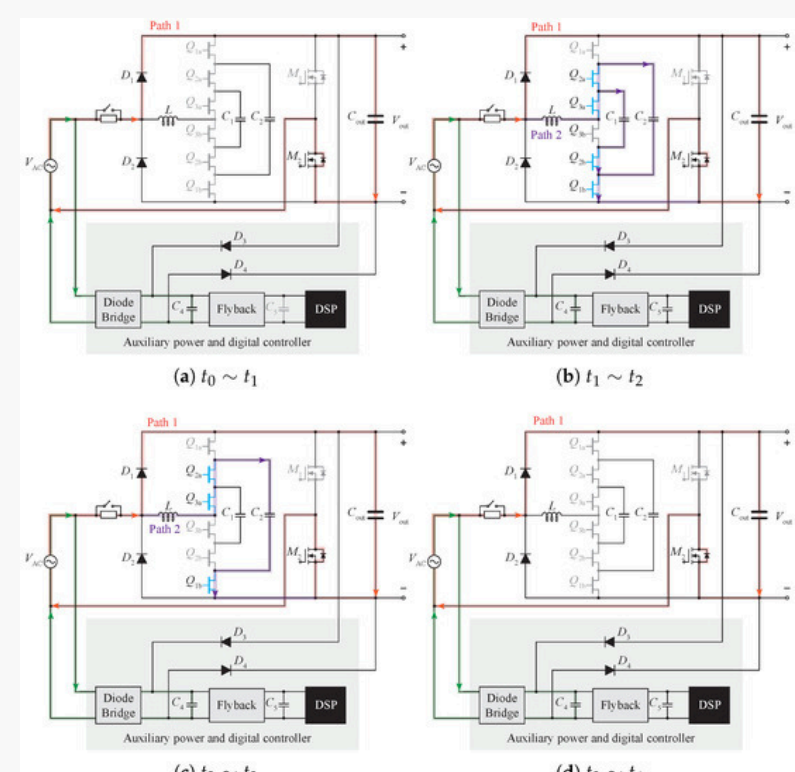
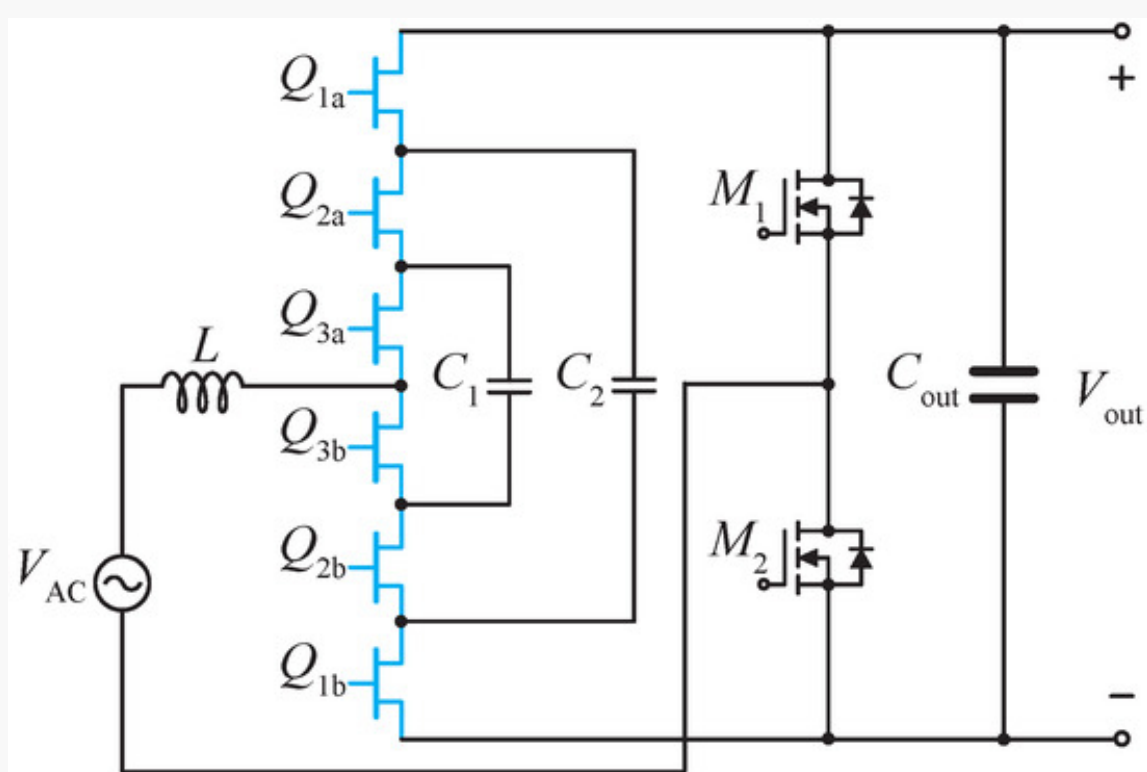


This paper explores the application of electromagnetic imaging techniques to characterize periodic rough surfaces. We introduce a DDCNN architecture designed to concurrently reconstruct the surface shape, identify the periodicity, and determine the dielectric constant. Through our numerical simulations, we demonstrate the effective reconstruction of periodic lengths, relative permittivities, and surface geometries across various configurations. Our findings underscore the significant impact of artificial intelligence on the reconstruction of a non-flat rough surface. During the training process, we discover that the DDCNN prioritizes the accurate determination of surface periodicity, followed by the estimation of dielectric constants and then the shape. It is worth mentioning that our method uses dilated convolution to effectively enhance the receptive field without incurring an additional computational burden, retaining the inherent advantages of traditional convolution. This prioritization is influenced by the varying sensitivities of each coefficient to the scattered field data, reflecting the intricate relationship between these parameters during the reconstruction process. In the future, we plan to integrate more advanced neural networks, such as Generative Adversarial Networks (GANs), alongside attention mechanisms, to enhance the reconstruction accuracy for complicated rough surface profiles. By repeatedly generating more realistic rough surfaces through GANs, it helps to improve the accuracy of reconstruction. The limitation of our proposal is that when the surface shape is too steep, the dielectric constant is too large, and when the period is too small, the reconstruction performance is affected. In three-dimensional scenes, the high computing cost will be a major challenge.

Multi-Path Precharge for GaN Flying-Capacitor-Multi-Level Totem-Pole PFC

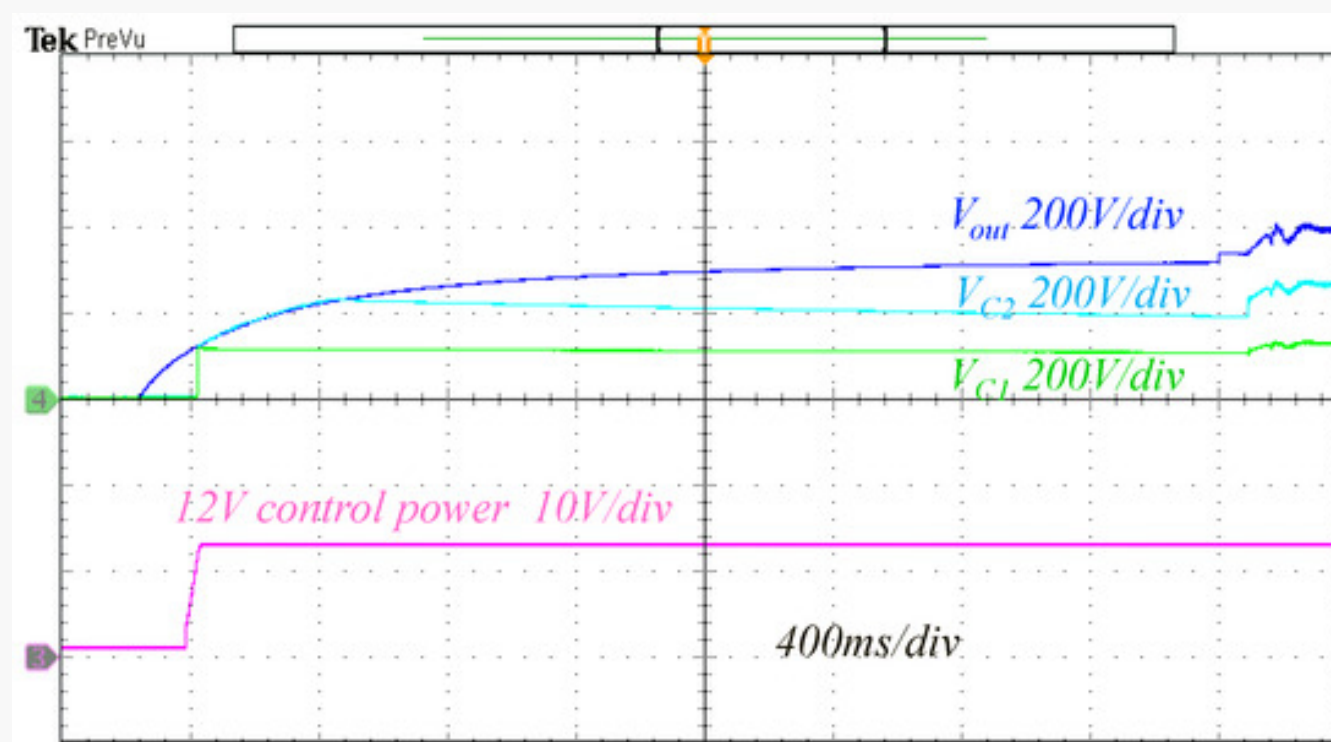
----- 24BFA04131- S Sai Nikitha

GaN flying-capacitor-multi-level (FCML) Totem-Pole power-factor-correctors (PFCs) have been demonstrated with very high density and efficiency in the literature. However, there is still a lack of detailed discussion about flying capacitor voltage precharge during the start-up for GaN FCML Totem-Pole PFCs. To enhance the reliability during start-up, we propose a multi-path and multi-step flying capacitor precharge method. In our proposed method, the bulky DC link capacitor is precharged through the path of the auxiliary line-frequency Si diode half-bridge and the body-diodes of the Si MOSFET half-bridge. The flying capacitors which have much smaller capacitances are precharged through the path of the GaN devices and the body-diodes of the Si half-bridge. The DC link capacitor is more than 100 times higher than the flying capacitor in this topology. Therefore, by splitting the total precharging current into two paths, the precharging current through the GaN devices is almost 100 times lower than that through the body-diodes of Si MOSFETs. As a result, this method protects expensive GaN devices from high inrush current and significantly improves the reliability of the GaN devices during the voltage precharge. Detailed operation principles and experimental verifications are presented in this paper.



GaN Totem-Pole Power-Factor-Correctors (PFCs) have been studied, demonstrated, and commercialized with more than 99% efficiency over the past few years. Combining a flying-capacitor-multi-level (FCML) converter and GaN Totem-Pole PFC to form a GaN FCML Totem-Pole PFC, has demonstrated a significantly higher efficiency and density. Therefore, GaN FCML Totem-Pole PFCs are high-efficiency and high-density PFC topology candidates for data centers, microgrids and smart grids. Due to the natural voltage balancing mechanism of the FCML converters.

The detailed circuit to limit the precharge inrush current, a current limiter is connected in series with the PFC main inductor. It will be bypassed by a relay when the precharge process ends. An auxiliary power circuit is designed and included in the system circuit, as well. The multi-step precharge method is proposed. The main concept is to use additional low-cost Si diodes to divert the huge inrush current for charging the bulky DC link capacitors from the high-cost GaN devices.



To verify the proposed multi-step and multi-path precharge method, we conducted detailed testing on a four-level GaN FCML Totem-Pole PFC. The specifications for the hardware are summarized. We used EPC2047 for the GaN device, which is a 200V/10mΩ device. The Si MOSFET is IPT60R028G7XTMA1, rated at 650V/28mΩ, whereby two such MOSFETs are used in parallel for M1 and M2. We used single-phase AC power source (Chroma 61605) and DC resistive load bank for testing. The experimental waveforms. From the tested waveforms, we can clearly see the flying capacitor and output capacitor voltages' precharging process.

In this paper, we proposed, developed and tested a multi-path and multi-step precharge method for GaN FCML Totem-Pole PFC. In the state-of-the-art precharge method, the GaN devices would be in the same charging path for charging the bulky DC capacitors, leading to a high inrush current through GaN devices. We propose to use two additional low-cost Si diodes to divert the high inrush charging current from the GaN devices. Therefore, the system has two precharge paths. One is through the Si diodes and the body-diodes of the Si MOSFETs, which are more than enough to handle the high inrush current for charging the bulky DC capacitors. The other path is through the GaN devices and the body-diodes of the Si MOSFETs to only handle very low inrush current for charging the very small high-frequency flying capacitors. The proposed method significantly improves the reliability of the high-cost GaN devices during the precharge process for GaN FCML Totem-Pole PFC.