SRI VENKATESWARA COLLEGE OF ENGINEERING
(Autonomous)
Karakambadi Road, Opposite LIC Training Centre, Tirupati – 517 507.
Accredited by NBA (B.Tech – CSE, ECE and EEE) & NAAC with 'A' Grade
Approved by AICTE, New Delhi permanently affiliated to JNTUA, Ananthapuramu.

FDPS, Workshops Organized by the Department- Consolidated Report

S.No	Name of the FDP/Workshop	Resource Person(s)	Date	No. of Days
2024-2025				
I Sem				
1	Hands-On-Training On Mixed VLSI System Design Using Cadence Tools	1. Dr.V. Prashanth, Assistant professor Department of Electrical Engineering, IIT Tirupati 2.T. Sudheer Kumar, Senior application engineer Entuple technologies pvt.ltd, Bangalore 3 M. Priyanshu, Senior application engineer Entuple technologies pvt.ltd, Bangalore.	2-12-2024 to 4-12-2024	3 Days
II- Sem				
2	Fundamentals and Emerging Trends in Internet of Things	1.Dr. S. Gokul, Professor, Department of ECE, I.I.I.T, Hyderabad. 2. Dr. B.R. Shivakumar, Professor, HOD of CSE, I.I.I.T, Hyderabad. 3. N. Thanuja, Lead project Coordinator, Infotech solutions. 4. M. Ramkumar Reddy, Team Leader, Infosys.	06-01-2025 to 10-01-2025	5 Days
2023-2024				
I -Sem				
3	Application ofEmbedded Systems to Internet of Things (AESIoT)	Mr. K.S. KAVIN, ME, MBA, (M.SC), (Ph . D), Founder and Managing Director, AB Technologies And AB Technologies Team.	01-08-2023 to 05-08-2023	5 Days
II-Sem				
4	Hands-On-Training on VLSI chip Design using CADENCE TOOL	1.Dr. Z. Abbas, Associate Professor, Department of ECE, I.I.I.T., Hyderabad. 2.Dr.K. Yajunath, Associate Professor, Department of ECE, N.I.E., Mysuru 3. Sandhya S, Physical Design Engineer, Intel, Bangalore.	19-02-2024 to 21-02-2024	3 Days
		2022-2023		
		I -Sem		
5	Recent Trends in Signal and Image Processing with hands-on training using MATLAB	1.Dr.V. Rajendran Dean R& D, VELTech, Chennai 2.Dr.P. Vijaya Lakshmi HOD ECE, I.I.I.T Hyderabad 3.P. Jerrita, Project Lead, Samsung Pvt.Ltd, Bangalore.	17-10-2022 to 21-10-2022	5 Days
II -Sem				
6	Hands-On-Training on VLSI Circuit Design (Analog/Digital) Using Cadence Suite	1. Kedharnath L V, ASIC Engineer, Entuple Technologies Pvt. Ltd., Bangalore. 2. P.Santosh Kumar,Physical Design Engineer, Cadence Design Systems, Bangalore. 3. K. Ramesh Gowda, Software Engineer, Cadence Design Systems, Bangalore	13-03-2023 to 15-03-2023	3 Days

Incharge **HOD**